UNIVERSITE LIBRE DE BRUXELLES

FACULTE DES SCIENCES

A VMEbus-Based Data Acquisition System for the Multiwire Proportional Chambers of the H1 Detector at the HERA Collider

Dissertation présentée en vue
de l'obtention du titre de
Docteur en Sciences

Philippe HUET

Mai 1993

UNIVERSITE LIBRE DE BRUXELLES

FACULTE DES SCIENCES

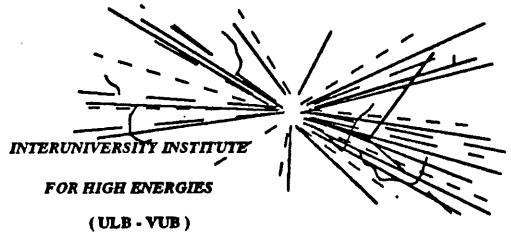
A VMEbus-Based Data Acquisition System for the Multiwire Proportional Chambers of the H1 Detector at the HERA Collider

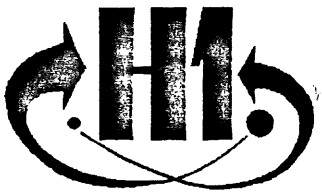
Dissertation présentée en vue
de l'obtention du titre de
Docteur en Sciences

Philippe HUET

Mai 1993

A VMEbus-Based Data Acquisition System for the Multiwire Proportional Chambers of the H1 Detector at the HERA Collider





Remerciements

Mes remerciements vont tout d'abord à Monsieur le Professeur Jean Sacton pour m'avoir offert la possibilité de travailler au sein de l'Institut Inter-universitaire des Hautes Energies pendant plus de 5 ans. Je lui suis très reconnaissant de m'avoir proposé un sujet qui m'a permis de m'initier aux techniques instrumentales et aux systèmes d'acquisition des données au sein d'un laboratoire de pointe. Son enthousiasme, ses conseils toujours pertinents, ainsi que la confiance dont il m'a toujours témoignée m'ont été d'un grand apport et m'ont encouragé à mener à terme ce travail.

Je tiens à exprimer ma plus grande reconnaissance au Dr. Robert Roosen dont l'intérêt constant pour mon travail a été une source continue de stimulation. Son soutien empreint d'amitié, ses conseils et suggestions, ainsi que l'aide qu'il m'a continuellement apportée ont été essentiels pour son bon aboutissement. Les nombreuses discussions que nous avons eues au cours de notre découverte de la gastronomie hambourgeoise ont été un divertissement apprécié et indispensable en certaines circonstances. Je tiens également à le remercier pour avoir bien voulu commenter et critiquer le manuscrit de cette thèse, bien que son contenu soit fort éloigné des sujets traditionnellement traités au laboratoire. Pour tout ceci, merci.

Mes remerciements vont aussi au Dr. Johan Morcels qui a développé le logiciel sans lequel aucune acquisition des données ne serait possible. En me faisant profiter de son expérience et de ses connaissances en programmation et en électronique il m'a beaucoup aidé. Sa persévérance a vouloir comprendre et résoudre les problèmes a été en particulier fort utile.

La réalisation d'une expérience de physique des hautes énergies est bien entendu le fruit d'un travail d'équipe. Au sein de l'IIHE, les Docteurs M. Barth, G. Bertrand-Coremans, D.P. Johnson et P. Marage n'ont jamais hésité à me donner une explication ou à m'apporter l'aide que je leur demandais. Je tiens également à remercier Erik Evrard qui connaîtra aussi très prochainement les joies de l'écriture. Pendant plus de trois ans, il a développé des logiciels permettant de tester le détecteur et les systèmes électroniques. Sa disponibilité et son ardeur au travail ont été grandement appréciés.

I would like also to express my gratitude to all my colleagues at DESY. It has been a pleasure working with them. I have benefited greatly from the advice and cooperation of too many engineers, physicists and technicians to list them individually. However I would thank by name Claire Bourdarios, Albrecht Leuschner, Katarina Müller and Stanislaw Mikocki who have actively participated in the installation and the tests of the MWPCs. Their friendship contributed greatly to the pleasant atmosphere within the group.

I also reserve special thanks for John Coughlan, Eckhard Elsen, Bill Haynes and Manfred Zimmer for their helpful advice and assistance during the implementation of the readout system. I am also indebted to Hanns Krehbiel, A. Hrisoho and Gisèle Martin for the many fruitful discussions about the front-end components.

Je n'aurais rien pu réaliser sans la collaboration efficace et toujours prompte de l'équipe d'électroniciens du laboratoire. Leur travail consciencieux, souvent sous-estimé, a été d'une importance cruciale à plusieurs moments. J'aimerais en particulier adresser mes plus vifs remerciements à Christian Wastiels et Rik Turtelboom pour leur très grand savoir faire tant dans leur travail que dans l'art de divertir au bon moment.

Enfin, ce document ne serait pas ce qu'il est sans le travail remarquable de Mesdames Danielle Luypaert et Myriam Pins. La qualité de la mise en page et des illustrations leur est entièrement due. Je tiens à les remercier très sincèrement pour l'aide qu'elles m'ont ainsi apportée et pour la patience dont elles ont fait preuve. Un très grand merci.

Pour terminer, j'aimerais citer quelqu'un qui a tout compris :

"Vous savez que j'ai un esprit scientifique.
Or récemment, j'ai fait une découverte bouleversante!
En observant la matière de plus près... j'ai vu des atomes... qui jouaient entre eux... et qui se tordaient de rire! Ils s'esclaffaient!
Vous vous rendez compte de conséquences incalculables que cela peut avoir?
Je n'ose pas trop en parler, parce que j'entends d'ici les savants: "Monsieur, le rire est le propre de l'homme!"
Eh oui!... Et pourtant! Moi, j'ai vu, de mes yeux vu, des atomes qui: "Ha, ha, ha!" Maintenant de qui riaient-ils?
Peut-être de moi? Mais je n'en suis pas sûr! Il serait intéressant de le savoir. Parce que si l'on savait ce qui amuse les atomes, on leur fournirait matière à rire... Si bien qu'on ne les ferait plus éclater que de rire.
Alors, me direz-vous, que deviendrait la fission nucléaire?
Une explosion de joie! "

Raymond Devos

Contents

List of Figures

List of Tables

Introduction

The last two decades have seen the construction of large particle accelerators providing collisions between leptons (LEP, SLC) or hadrons (Sp$\bar{p}$S, TEVATRON). In 1991, the world's first lepton-hadron collider has been commissioned at the Deutsches Elektronen-Synchrotron (DESY) in Hamburg. The Hadron Elektron Ring Anlage - HERA - is designed to collide 820 GeV protons and 30 GeV electrons resulting in a center of mass energy of $\sqrt{s} = 314\ GeV$. The design luminosity is 1.5 $10^{31}\ cm^{-2}s^{-1}$. This new collider offers the possibility to greatly extend our knowledge in the field of deep inelastic lepton-nucleon scattering. HERA increases the accessible kinematic range to values of $Q^2 \sim 4\ 10^4\ GeV^2$ both for neutral and charged current scatterings, i.e. 2 orders of magnitude higher than at previous fixed target experiments.

At the present time, two general purpose detectors are operational at HERA : H1 and Zeus. A third experimental apparatus, the HERMES detector, is proposed to measure the spin dependence of the nucleon structure functions with longitudinally polarised electrons. The H1 and Zeus experiments have collected their first data during the period from June through November 1992. At that time the accelerators collided beams of 26.7 GeV electrons with 820 GeV protons at about 2 permile of the design luminosity. The next run is currently scheduled to begin in June 1993.

HERA presents a technical challenge for both the detectors and the data acquisition systems that is unique within the High Energy Physics environment. To operate at the design luminosity, 210 electron and proton bunches are used, providing a new crossing every 96 ns, i.e. approximately 100 times more frequent than at LEP. For the first time, data have to be tested for possible triggers at an input rate of 10^7 MHz without impeding the system with a large dead time. This requires a novel approach to data acquisition and trigger processing. For instance, the first level trigger has to work in a pipelined mode and storage elements have to be provided for every detector channel before hardware and software processing. Synchronization between the various system components is a major issue that deserves special consideration. In this context, the experience gained at HERA regarding triggering techniques and data processing certainly forms an important input to the design of front-end data acquisition systems for the next generation high rate hadron colliders.

The work presented in this thesis concerns the data acquisition system used to readout the data of all the multiwire proportional chambers (MWPC) in the H1 detector. As a member of the H1 collaboration since 1987, I took an active part in the design, the development and the commissioning of this system. My main responsibilities consisted in the conception and the development of the front-

end data acquisition system based on an inter-crate connection which transfers the buffered front-end data into a memory accessible to the central DAQ system. These transfers are executed by a DMA controller without processor intervention making use of on-board FIFO buffers. I furthermore designed the printed circuit boards that hold the preamplifiers for the Central Outer Proportional chamber and was deeply involved in the tests of the front-end electronics. During the commissioning phase, I was responsible for the implementation of the MWPC readout system at the DESY laboratory.

Chapter 1 describes the experimental framework. An overview of the HERA collider and its injection system is first given. Next, the major criteria that must be taken into account when designing an experiment at HERA are considered. The kinematics of e-p interactions are briefly reviewed followed by a short discussion of event signatures. The problem of the determination of the bunch crossing time is introduced. The last section describes the H1 detector with special focus on the tracking system.

Chapter 2 describes the H1 data acquisition system in general. An overview of the principal parameters which have determined the system architecture is first presented. In particular the bunch crossing rate, the event rate, background rates and the data volume are discussed. Furthermore, an overview of the H1 trigger system is presented followed by a description of the consecutive steps of the acquisition procedure. Hardware details are outlined in the last section with an introduction to the VMEbus specification as well as a description of the major front-end systems and of the central data acquisition.

Chapter 3 describes the analog signal processing in the MWPC system. The principles of particle detection in multiwire proportional chambers are first reviewed together with a description of the pad readout technique used for the central and forward MWPC detectors. Subsequently, the front-end electronic chain is outlined including in particular a description of the preamplifier, the shaper and the Receiver Card.

Chapter 4 is devoted to the Receiver Card readout system. Its general structure is first presented together with a description of the data flow through the different buffering stages. Then, the data acquisition modules are reviewed. The custom-built components are described in some detail with a particular attention to those related to the inter-crate connection. The synchronization mechanisms are then presented. The logic used to control the front-end synchronizer and pipeline is first described followed by the interrupt protocol used for controlling the readout tasks. The performance of the system is analysed in terms of its data transfer rate dead time.

Finally, a summary of the main characteristics of the system is given and the general conclusions are drawn.

Chapter 1

H1 at HERA : The Collider and the Experiment

1.1 Introduction

High energy lepton-nucleon scattering has played an essential role in our understanding of the constituents of matter and their interactions. The early deep inelastic electron scattering experiments at SLAC revealed the parton structure of the nucleon. Since then many further insights have been provided by experiments using neutrino and muon beams. For instance, the existence of the weak neutral current interaction was first demonstrated in 1973 at CERN in $\nu_\mu p$ scattering processes. These observations were the experimental foundation of quantum chromodynamics (QCD), the gauge theory of strong interactions.

This line of research is now continued at the new and first electron-proton collider HERA at DESY that allows collisions between 820 GeV protons and 30 GeV electrons. This facility opens a new kinematical region for physics measurements inaccessible to fixed target experiments. At HERA, the momentum transfer squared between the electron and the proton can reach a value as large as $Q^2 \sim 4\ 10^4\ GeV^2$, i.e. about 2 orders of magnitude higher than at the CERN and FNAL fixed target experiments. For the first time, lepton-nucleon scattering events are studied at momentum transfers comparable with the rest masses of the $W^\pm$ and Z^0 gauge bosons, where the weak and electromagnetic interactions are of comparable strength. The simultaneous measurement of charged current and neutral current cross sections offers the possibility to perform precision tests of the Standard Model and to eventually establish deviations from the theory. With HERA, it will be possible to probe the electron and the quarks down to distances of $\sim 10^{-18}$ m and search for possible sub-structures at dimensions which are an order of magnitude smaller than possible with present-day accelerators. A detailed

view of the physics program at HERA is presented in [1] and [2].

To study e-p interactions at HERA, two large complex detectors, called H1 and ZEUS, have been installed at two interaction points. In these detectors, the reaction products from head-on collisions between electrons and protons circulating in opposite directions in the storage rings are measured and recorded. The design and construction of these two devices result from a common effort of about 550 physicists and engineers from 16 countries. The Interuniversity Institute for High Energies ULB/VUB figures as one of the participating institutes of the H1 collaboration. Its hardware contribution consists in the construction of the Central Outer Proportionnal Chamber (COP), one of the components of the H1 track detector, and the development of the readout electronics of the MWPC detection system.

In this chapter, an overview of the HERA collider and the H1 experiment is presented. In the first section, the HERA rings and the preaccelerator complex are described. Next, experimentation at an e-p collider is discussed, before describing the H1 detector. We will then focus on the tracking devices and more particularly on the COP detector.

1.2 The HERA Collider

1.2.1 Introduction

The Hadron Elektron Ring Anlage (HERA) consists of two separate 6.3 km long rings, designed to accelerate and to store respectively 820 GeV protons and 30 GeV electrons (positrons) and to allow the collision of the two counterrotating beams head on in four interaction points [3]. The layout of HERA with its injection system is shown in Fig 1.1. The main parameters are listed in table 1.2.

At the nominal beam energies, the center of mass energy is

$$\sqrt{s} \simeq \sqrt{4E_e E_p} = 314\ GeV \tag{1.1}$$

equivalent to an electron beam of 51 TeV incident on a stationary target. The design luminosity is 1.5 10^{31} cm^{-2} s^{-1} leading to data samples of typically 100 - 200 pb^{-1}/year. To obtain this luminosity, both beams are bunched in 220 equidistant buckets, out of which 210 are filled with particles, providing a crossing every 96 ns. This time is much shorter than the beam crossing time at the present day accelerators and approaches the bunch separation at the future hadron colliders (see table 1.1.).

Collider	*Type*	Δt
LEP	e^+e^-	11 μs
TEVATRON	$p\bar{p}$	3.2 μs
HERA	e-p	96 ns
LHC/SSC	pp	15/16 ns

Table 1.1: Time between bunch crossings at existing and futur colliders.

HERA will provide the possibility to collide the protons with longitudinally polarized electrons or positrons. This offers the opportunity to do experiments with predominantly left or right handed $e^{\pm}$ and opens new possibilities in the investigation of the chiral structure of the gauge interactions.

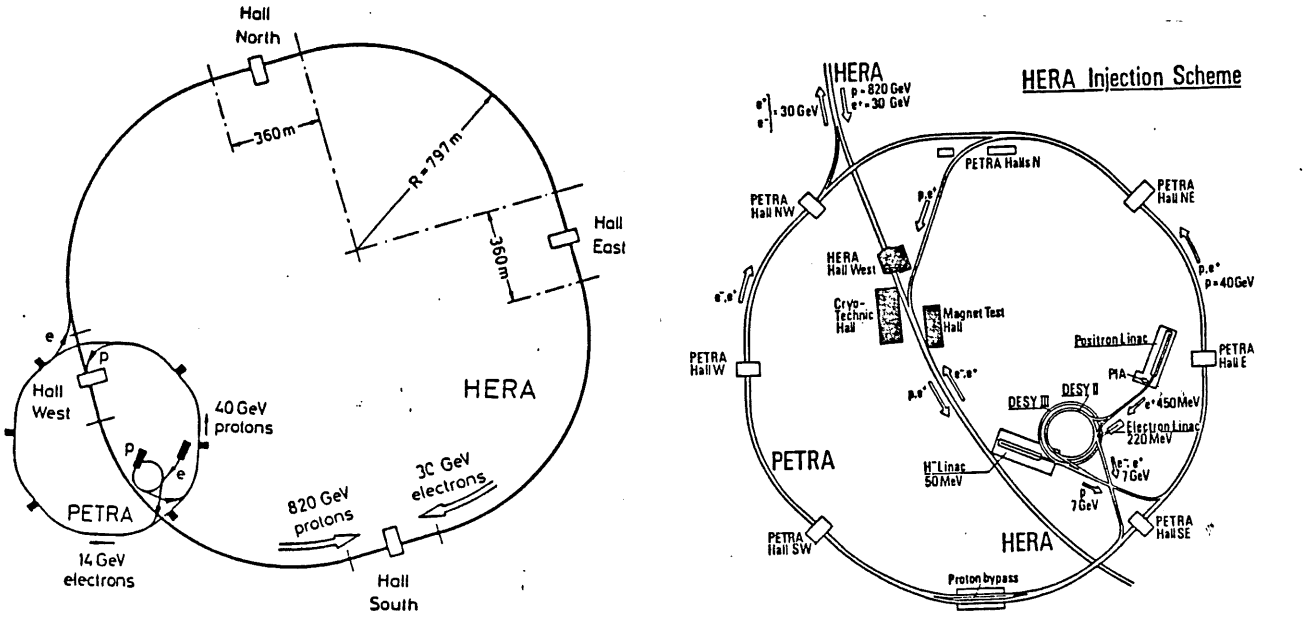


Figure 1.1: Layout of HERA and its preaccelerators

1.2.2 The Injection Systems

The electron injection system of HERA is based on the rebuilt Deutsches Elektronen-Synchrotron (DESY) and the modified storage ring PETRA previously used for e^+e^- collisions. The electrons from a 500 MeV linear accelerator are injected into a small storage ring where they are accumulated into a 60 mA single bunch. They are then injected into the synchrotron DESY II, accelerated to 7 GeV, and transferred to the PETRA ring. After accumulating up to 70 bunches with the final

bunch spacing of 28.8 m, the PETRA energy is ramped up to 14 GeV and at that energy, the bunches are transferred to HERA. This process is repeated until HERA is filled with 210 bunches.

	p-ring	*e-ring*	*units*
Nominal energy	820	30	GeV
Polarization time		28	min
Luminosity	1.5×10^{31}		$cm^{-2}\ s^{-1}$
Space between IR Quad	15		m
Interaction points	4		
Crossing angle	0		mrad
Circumference	6336		m
Magnetic field	4.68	0.165	T
Number of particles	2.1	0.8	10^{13}
Number of bunches	210		
Injection energy	40	14	GeV
Filling time	20	15	min
σ_x/σ_y at I.P.	0.29/0.07	0.26/0.02	mm
σ_z at I.P.	110	8.0	mm
Energy loss / turn	6.24×10^{-6}	127	MeV
Circumferential RF Voltage	0.2/2.4	260	MV
RF-Frequency	52.033/208.13	499.776	MHz
RF-power	1	13.2	MW
Refrigerator	21.0 kW (isothermal at 4.K) 60 g/s Liq. He 60 kW (40 K - 80 K)		

Table 1.2: General parameters of HERA

The proton injection complex is based on a whole new chain of preaccelerators. Negatively charged hydrogen ions are first accelerated to 750 KeV and then injected into a 50 MeV linear accelerator. The H^- ions are stripped upon entering into the synchrotron DESY III where they are captured into 11 RF buckets with the final bunch spacing. The protons are then accelerated to 7.5 GeV and transferred to PETRA. After filling with at most 70 bunches, the protons are accelerated to 40 GeV and the train of bunches transferred to HERA.

The total filling time is expected to be 15 min. for the electrons and 20 min. for the protons.

1.2.3 The HERA Rings.

1.2.3.1 The Electron Ring.

For 30 GeV electrons, a modest bending field of 0.165 T is required and can be achieved with conventional magnets. The energy lost by synchrotron radiation (127 MeV/turn at E = 30 GeV) is compensated by 500 MHz RF cavities located along the electron beam. HERA is equipped with 83 such cavities, previously used at PETRA, and 8 additional superconducting cavities to reach the nominal energy of 30 GeV.

1.2.3.2 The Proton Ring.

To keep the 820 GeV protons on orbit, a bending field of 4.68 T and a quadrupole gradient of 90 T/m are required. For this purpose, a new design of superconducting Nb-Ti magnets was devised in which the iron is at liquid He temperature. To obtain the required field uniformity, a mechanical precision of 20 μm on the conductor location had to be maintained over the 9 m dipole length. The quadrupole and sextupole correction magnets are also superconducting, whereas normal conducting magnets are used to guide the protons in the four straight sections. The quality of the magnets is such that at 4.6 K, the quench occurs at 5.8 T and operation at 1 TeV is not out of the question. As the energy loss due to synchrotron radiation is negligible for protons, conventional RF cavities and klystrons are used.

1.3 Experimentation at HERA

To study e-p interactions at HERA, two general purpose detectors, H1 and Zeus, have been built. Before describing the H1 detector, let us consider the major criteria that have to be taken into account when designing experiments at HERA.

1.3.1 Kinematics

The dominating interactions at HERA are the neutral current (NC) scattering process $ep \rightarrow eX$ and the charged current (CC) process $ep \rightarrow \nu_e X$. Figure 1.2 shows the relevant Feynman diagrams that describe, at the lowest order, these classes of interactions.

In the parton model of the proton, the incoming electron interacts directly with one of the quarks inside the proton via a spacelike neutral (γ/Z^0) or charged

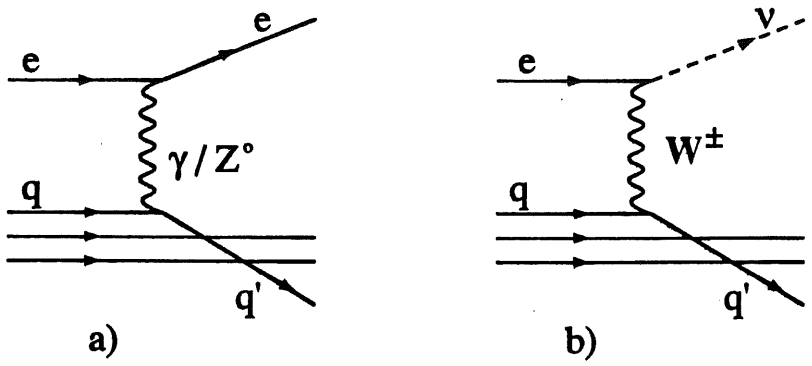


Figure 1.2: Feynman diagrams for neutral (a) and charged (b) current e-p interactions

($W^{\pm}$) current. The struck quark will materialize as a jet (current jet) of hadrons whose transverse momentum p_t is balanced by the scattered lepton. Occasionally, the quark will radiate a high energy gluon that gives rise to a well separated two jet structure (gluon jet and quark jet) in the current fragmentation region. The remainder of the proton will appear as a sharply collimated jet (target jet) of hadrons leaving the interaction region in a narrow cone ($\sim$ 10 mrad) around the proton beam direction (see figure 1.3).

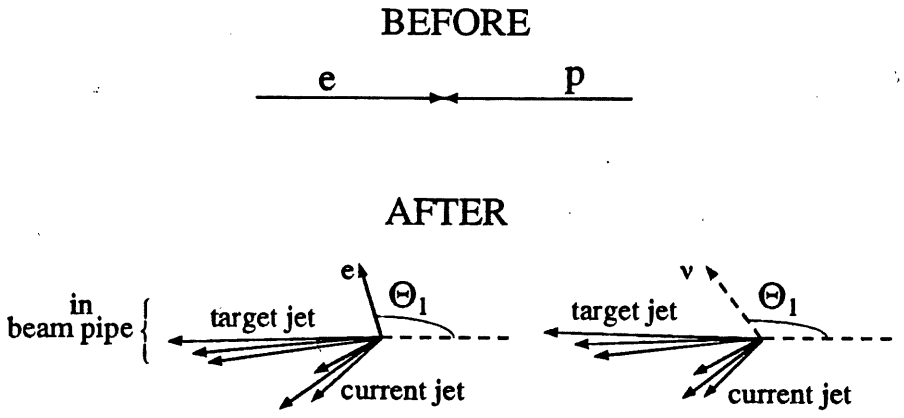


Figure 1.3: Topology of deep inelastic e-p scattering events

To give the basic kinematical expressions,let p_e, p_l, E_e, E_l be the four-vectors and the energies of the incoming and scattered leptons, P the four-vector of the incoming proton, and Θ_l the scattering angle of the outgoing lepton. The total mass squared is

$$s = (p_e + P)^2 \simeq 4E_eE_p \tag{1.2}$$

where the sign "$\simeq$" means that the lepton and proton masses are neglected with respect to energies in the laboratory frame [4].

The Q^2 variable is defined to be minus the square of the four-vector $q = p_e - p_l$ of the exchanged boson :

$$Q^2 \equiv -q^2 = -(p_e - p_l)^2 \simeq 4\ E_e E_l \sin^2 \frac{\Theta_l}{2} \tag{1.3}$$

The energy transferred to the hadronic final state in the proton rest frame, defined as ν, is given by the relation :

$$m_p \nu \equiv P \cdot q \simeq 2E_p(E_e - E_l \cos^2 \frac{\Theta_l}{2}) \tag{1.4}$$

Let us now define the convenient dimensionless Bjorken - x and y variables:

$$x \equiv \frac{Q^2}{2P \cdot q} \simeq \frac{E_e E_l \sin^2 \frac{\Theta_l}{2}}{E_p(E_e - E_l \cos^2 \frac{\Theta_l}{2})} \tag{1.5}$$

$$y \equiv \frac{P \cdot q}{P \cdot p_l} \simeq \frac{E_e - E_l \cos^2 \frac{\Theta_l}{2}}{E_e} \tag{1.6}$$

with

$$Q^2 = sxy \tag{1.7}$$

These variables are always in the range $0 \leq (x, y) \leq 1$ and are independent of any proton or electron model assumption. By assuming the quark-parton model, where the current couples to a quark, and assuming the initial and final quark to be massless, the Bjorken-x variable can be interpreted as the momentum fraction of the proton carried by the struck quark. However, taking QCD corrections into account this interpretation no longer holds [5].

Any two of the above variables can be used as independent variables to describe the phenomenology of the e-p interactions. The couples (x, y) and (x, Q^2) are most commonly used. Figure 1.4 shows the experimentally accessible regions at HERA and in the present fixed target experiments. There is about an order of magnitude in Q^2 between the end points of both domains. Some overlap may be established by running the HERA accelerators at lower energies. HERA extends the kinematical range by two orders of magnitude down to values of $x = 10^{-4}$. This small x region may be viewed as the fixed target region of HERA where the struck quarks are almost at rest. There is a strong interest to investigate these events because at very low values of x and large values of Q^2, the parton density in the nucleon is expected to grow rapidly leading to possible interactions between the partons. New physics phenomena are therefore expected in this domain which could lead to corrections in the perturbative QCD theory.

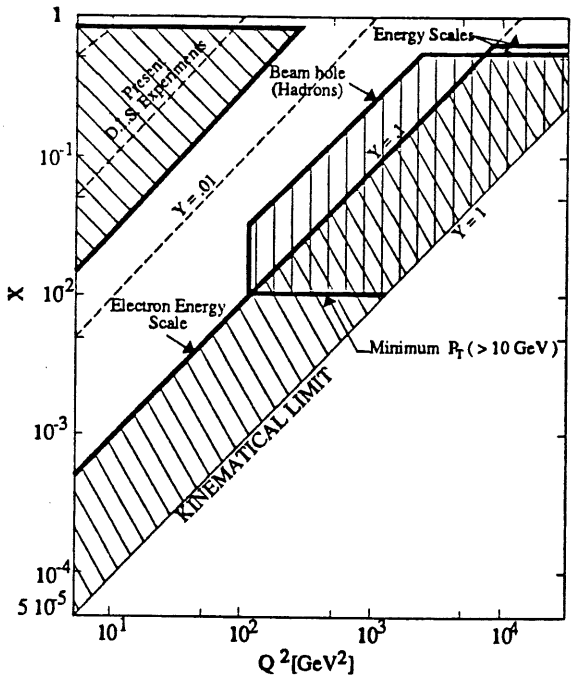


Figure 1.4: Experimentally accessible regions for structure function measurements at HERA nominal beam energies of 30 GeV electrons and 820 GeV protons. The domains covered by vertical and 60° hatched lines specify the regions where differential cross-sections are expected to be measurable with less than 10% systematic errors from the reconstruction of the visible hadron flow and the scattered electron, respectively. Taken from [6].

1.3.2 Event Signatures

From the experimental point of view, the variables x, y and Q^2 can be determined in neutral current events from the energy E_l of the outgoing lepton and its scattering angle θ_l by using equations 1.3, 1.5 and 1.6. These events are characterised by an isolated high energy electron (E$\geq$ 30 GeV) balanced in p_t by the jet(s). On the other hand, a charged current event is signaled by high p_t jet(s) with missing transverse energy due to the non detection of the emitted neutrino. In that case, only the information from the hadron system can be used. The above variables must then be expressed in terms of the total current jet energy E_j and of the polar angle θ_j. This method requires that one disentangles particles of the current jet from particles of the target jet, which in practice may well be impossible. To overcome this problem, A. Blondel and F. Jacquet have proposed a method to determine the kinematical variables in charged current events based on measured quantities summed over the complete hadron system [7] :

$$y = \sum_{h(all\ hadrons)} \frac{(E_h - p_{zh})}{2E_e} \tag{1.8}$$

$$Q^2 = \frac{P_t^2}{(1-y)} = \frac{|\sum \vec{p}_{th}|^2}{(1-y)}, \quad x = \frac{Q^2}{sy} \tag{1.9}$$

where P_t is the total transverse momentum of the hadron flow, p_{zh} the longitudinal momentum component and $\vec{p}_{th}$ the transverse momentum of the hadron h. In these equations, the contribution of particles going into the beam hole is small relative to the contribution of particles with larger Θ. For $x < 0.5$ and $Q^2 > 100GeV^2$, the relative errors in x and Q^2 remain below 10% [8].

The physics topics outlined above demand the following main detector components:

- a high quality hadron calorimetry for precise energy flow measurement, combined with an electromagnetic calorimeter to identify and to measure the scattered electrons. A high degree of hermiticity is needed to minimize any missing energy.
- a track detector operating in a magnetic field for particle emission angle and momentum measurements and for particle identification by a dE/dx measurement.
- a muon detector for a correct determination of the total visible energy since muons deposit only a fraction of their energy in the calorimeter. With the electrons, the muons are expected to provide signatures for new phenomena involving heavy flavours and new particle production. They will be identified by their penetration through the absorption materials of the detectors and measured by tracking chambers situated outside of the other detector subcomponents.

1.3.3 Determination of the Bunch Crossing Time

The 96 ns time separation between bunch crossings imposes several constraints on the design of a detector at HERA. Most of the usual detector components have a charge collection time which is much larger than 96 ns. For instance, the signals from the H1 calorimeter have a length of about 500 ns and the maximum drift time in the tracking chambers approaches $2\mu s$. This means that the signal processing time for a particular event has to be at least of this duration to measure all deposited charge. As a consequence, events arising from consecutive interactions may overlap during the resolving time of the detector. It is therefore essential to be able to determine uniquely to which HERA beam crossing each detector signal is associated. An erroneous bunch-event association would result in wrong drift distances and particle energies.

The determination of the beam crossing time requires devices which can correlate the data from the different parts of the detector with a specific bunch crossing.

For this purpose, multi-wire proportional chambers may be used. Provided a small wire spacing (typically 2 mm) and a suitable gas are chosen, the drift time will be much smaller than 96 ns and simple discrimination on the chamber pulses will define uniquely the bunch crossing time t_0. Bunch crossing identification is also possible with detector components which do not have single bunch crossing response times. For instance, the arrival time of liquid ionization calorimeter signals can be derived from the zero-crossing of their predictable pulse shape [9].

1.4 The H1 Detector

H1 is a general purpose detector for HERA designed to measure with high precision particles and jets with energies up to 820 GeV. The detector has been optimized for the study of neutral and charged current interactions and, in particular, for the measurement of the energy and momentum of single electrons. The overriding design goal has been a large, finely grained, calorimeter covering nearly 4π, enhanced by tracking and particle identification elements. As in e-p interactions, the track densities and particle momenta are much larger in the forward (proton) direction than in the barrel and backward (electron) regions, the detector has an asymmetric shape. A view of the detector is presented in figure 1.5. A brief overview of the detector components is given below, followed by a more detailed description of the tracking detector which includes the multiwire proportional chambers.

1.4.1 Detector Scheme

The heart of the H1 detector [9] is a liquid argon (LAr) calorimeter covering the forward ($4^\circ < \Theta < 20^\circ$) and central ($20^\circ < \Theta < 152^\circ$) detector regions. It is composed of an electromagnetic section (4), with 2.4 mm thick lead absorber plates and 2.35 mm argon gaps, and a hadronic section (5) with stainless steel plates of 19 mm thick combined with a double gap of 2×2.3 mm argon. The depth of the electromagnetic section varies between 19 and 30 radiation lengths while the hadron containment is obtained with 4.7 to 8 absorption lengths of LAr stacks. Both parts are welded together within a single vacuum insulated cryostat.

The liquid argon technique allows for a fine readout segmentation both transverse and longitudinal to the beam axis. Transversely, the granularity varies between 10 and 100 cm^2 in the electromagnetic calorimeter and between 50 and 2000 cm^2 in the hadronic part. Longitudinally, the electromagnetic shower is sampled 43 to 119 times, the hadronic shower 16 to 36 times. This fine segmentation allows to correct for the different electromagnetic and hadronic responses and consequently improve the energy resolution. This is done by a weighting algorithm applied to the individual longitudinal and transverse energy distribu-

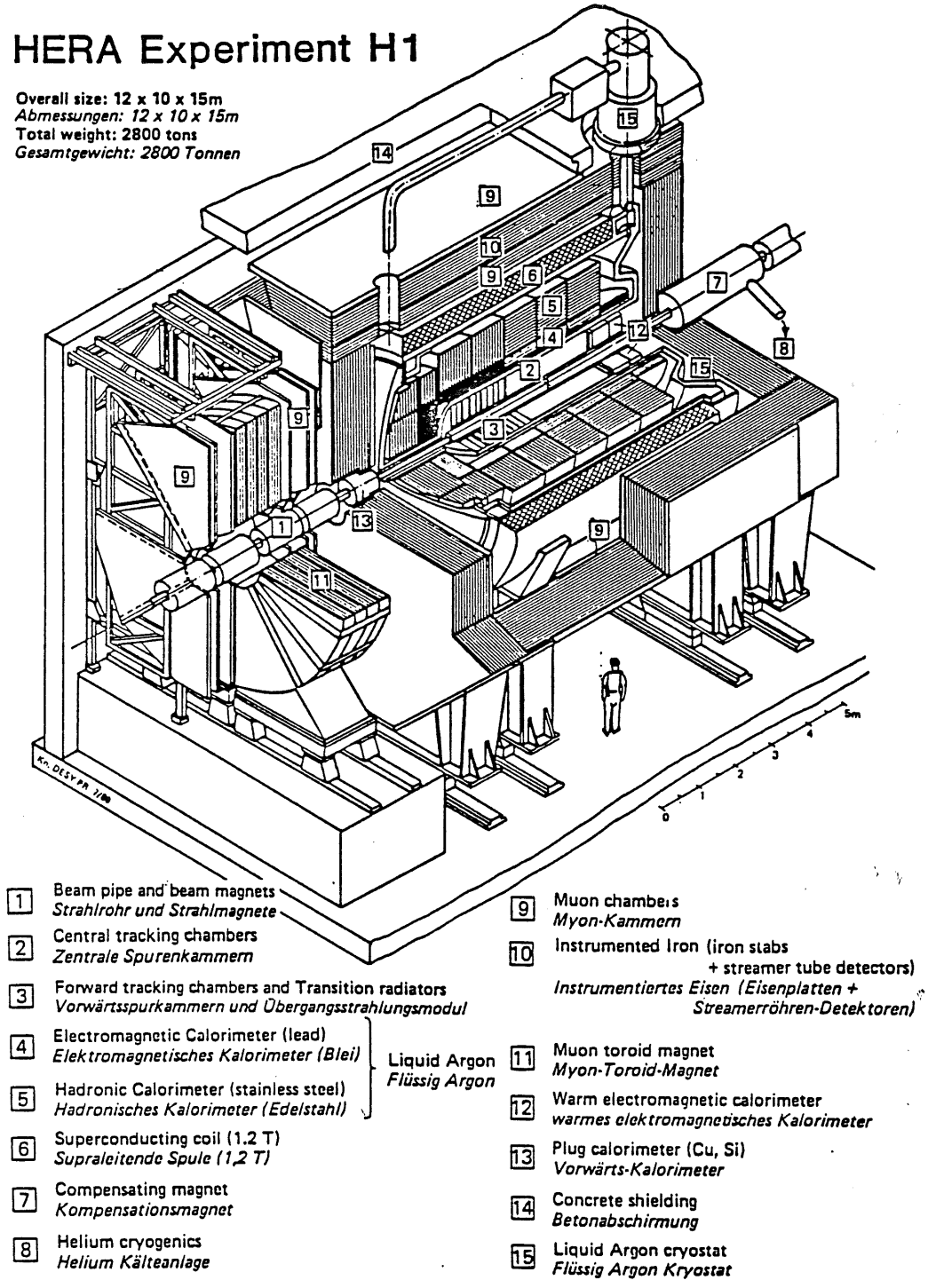


Figure 1.5: The H1 detector

tions which equalises the relative responses of electrons and photons with the hadron one. After this correction, an energy resolution for hadronic showers of $\sigma(E)/E = 0.50/\sqrt{E(\mathrm{GeV})}$ is achieved. The electromagnetic energy resolution is $\sigma(E)/E = 0.12/\sqrt{E(\mathrm{GeV})}$.

The LAr calorimeter is completed in the backward direction by an electromagnetic calorimeter (BEMC) which covers the angular range $151° < \Theta < 176°$ (12). It is a lead-scintillation sampling calorimeter with photodiode readout. The energy resolution for the electrons is approximately the same as for the liquid argon calorimeter. In the forward region, a plug calorimeter (13) covers the angular range $12.5\ mr. \leq \Theta \leq 60\ mr.$ and measures the hadronic energy flow which escapes the LAr calorimeter. It is made of copper absorber plates sandwiched with silicon detectors.

Charged particle tracking is provided by a set of drift chambers inside the calorimeter. In the central region, the tracker (2) consists of a central jet chamber interleaved with 2 layers of z-drift chambers and multiwire proportional chambers (MWPC). In the forward region, a series of radial and planar drift chambers, interleaved with MWPCs and transition radiators, are installed (3). In the backward region, four layers of MWPCs close the tracking detector. This system is described in more detail in the next section.

A Time of Flight (TOF) device consisting of a double wall of scintillators is installed inside the tracker tank immediately behind the BEMC. It is used to generate a veto on background particles travelling with the beam (halo, beam-gas or beam-wall collisions).

The detector components discussed so far are installed inside a superconducting coil (6) and operate in a longitudinal magnetic field of 1.2 T. Around the solenoid, an iron structure (10) acts as the return yoke for the magnetic field. It is fully instrumented with gas counters, operating in the limited streamer mode, to measure the hadronic energy leaking out the main calorimeter (tail catcher) and to detect the muons. This system is supplemented in the proton direction by a muon spectrometer composed of a iron toroid (11), with a field of 1.2 T, and four layers of drift chambers.

In the electron direction, two large VETO walls made of scintillator counters are placed at z = - 6.5 m and z = - 8 m from the interaction point. They are used to identify penetrating particles produced upstream in the proton beam line in beam-gas and beam-wall interactions and the shower leakage in the beam pipe from the e-p interactions.

In the same direction, a photon and an electron detector are placed at small angles located at distances of about 107 m and 37 m. These detectors measure the luminosity and tag interactions with small momentum transfer. Each com-

ponent consists of a crystal calorimeter with an energy resolution of $\sigma(E)/E = 0.12/\sqrt{E(GeV}$. The luminosity is determined using the Bremsstrahlung process $e + p \rightarrow e + p + \gamma$ in which the energy of the electron and the photon are measured. As the electron beam-gas interaction produces also Bremsstrahlung, a subtraction is made by measuring this component with noncolliding electron bunches.

1.4.2 Tracking Detectors

1.4.2.1 Introduction

The tracking system of the H1 detector is located within the cryostat of the LAr calorimeter. Its layout is shown in figure 1.6. Due to the particular event topology of e-p collisions, the tracker is subdivided into two parts, the central track detector (CTD) and the forward track detector (FTD) :

- The CTD covers the angular region $25° < \Theta < 160°$. It consits of two jet chambers (CJC1, CJC2) interleaved with 2 sets of z-drift chambers (CIZ, COZ) and MWPCs (CIP, COP).
- The FTD occupies a cylindrical volume in the proton direction ($5° < \Theta < 25°$) where over 50% of the particles are expected to enter. It is constructed as a set of 3 identical subunits (supermodules) which repeat along z. Starting from the interaction point, each supermodule contains one planar drift chamber, followed by a MWPC plane, then a transition radiator and finally a radial drift chamber.

The drift chambers of the tracking system have been designed to reconstruct jets with high particle densities. A double-track resolution of about 2.5 mm is obtained and momenta and angles of scattered electrons are measured to a precision of $\sigma_{p_t}/p_t^2 \leq 0.003\ GeV^{-1}$ and $\sigma_\Theta \sim 1$ mrad. They also improve the e/π separation of the calorimeter by providing electron identification by means of ionisation loss (dE/dx) measurement and detection of transition radiation.

The system of MWPCs is used for fast timing and to provide prompt track information for building customized ray triggers. It is the only large solid angle subdetector which has a charge collection time shorter than the 96 ns interval between beam crossings. The chambers provide for each event a precise determination of the interaction time t_0. They have a two dimensional pad readout and consequently provide genuine space points of the charged particle tracks which are used to define rough trajectories. The dimension of the pads along the beam axis and the circumferential segmentation have been optimized to ensure a vertex

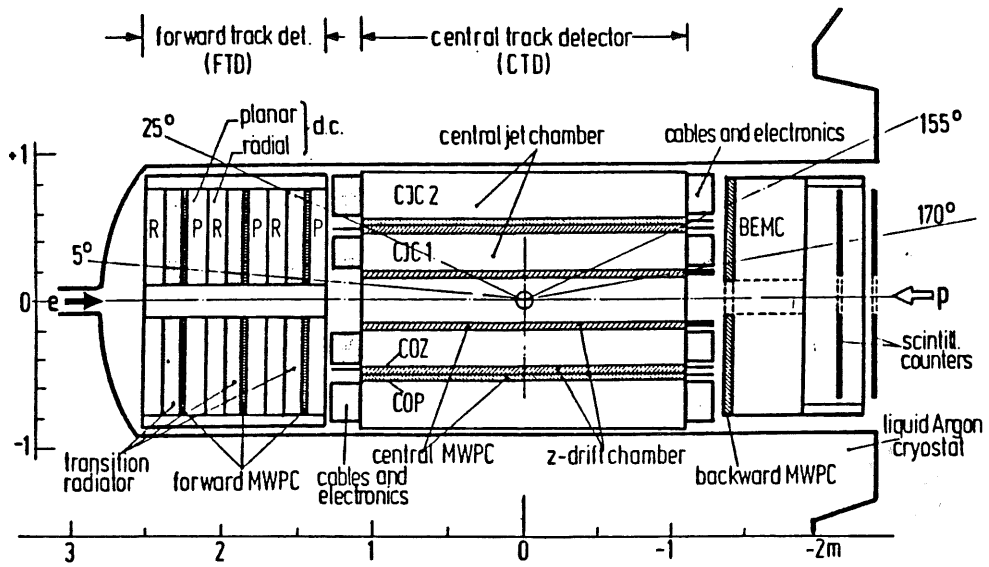


Figure 1.6: The H1 tracking system

resolution along the beam of 5 cm and to allow coincidences between the MWPC rays and the corresponding calorimeter signals. The use of the MWPCs in the trigger system is described in chapter 2.

The backward region is covered by an additional MWPC (BPC) with 4 wire planes rotated by 45° with respect to one another. The wire readout of this chamber provides one space point per track up to angles of $\Theta = 175°$. This information is used to measure, with the central inner track detectors, the Θ-coordinate of particle tracks hitting the backward electromagnetic calorimeter, e.g. electrons from low x neutral current events, and for e/γ separation in the BEMC.

1.4.2.2 Central Tracker

The central tracker is based on two jet chambers (CJC1 and CJC2) that provide for charged particles an accurate measurement of the $r\phi$-coordinates ($\sigma_{r\phi} = 210\ \mu$m) and a moderate measurement of the z-position ($\sigma_z \sim 25\ mm$). The CJC detectors [10] are cylindrical drift volumes centered around the beam pipe with the wires running parallel to the beam axis. They are divided respectively in 30 and 60 jet cells separated by planes of cathode wires (fig. 1.7). Each cell consists of 24/32 sense wires alternating with two potential wires. The maximum drift distance is 44.5 mm which results in a drift time of about 1.2 μs, assuming a drift velocity of 40 μm/ns. The jet cells are tilted by $\pm$ 30° with respect to the radial direction in order to compensate the deflection of the electron drift trajectory in the magnetic field of 1.2 T. As a consequence, the secondary electrons drift approximately perpendicular to the high momentum tracks so that the resolution is

optimized. Another advantage is that all tracks above a minimum transverse momentum ($\geq$ 100 MeV/c) traverse at least one sense wire plane which means that at least one drift time is shorter than 96 ns. This allows a separation of tracks coming from different bunch crossings and the use of the drift chamber information in a fast trigger logic.

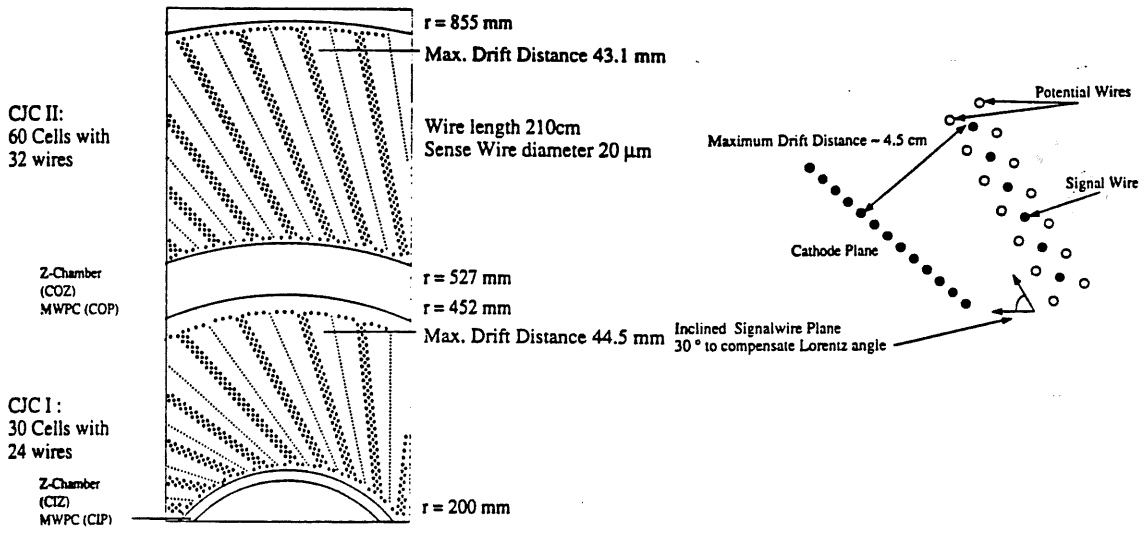


Figure 1.7: Central tracker, section perpendicular to the beam with details of the CJC cell structure

All sense wires of the CJCs are read out independently on both sides by a chain of preamplifiers and analog-to-digital converters (see 2.5.3). On average 56 space points are measured on a track over a length of $\sim$ 650 mm. The total number of channels is 5280.

A precise determination of the z-coordinate is obtained from two z-drift chambers located at radii of 200 mm (CIZ) and 470 mm (COZ). These chambers [11], [12] are made of rings along the z-axis divided axially into rectangular drift cells. In each ring there are four layers of sense wires alternating with guard wires which are strung around the circumference of the chamber. In the cells, the electrons drift along the z-axis in the electric field produced by a series of cathode strips. The drift lengths are confined to 5.9 cm (CIZ) and 4.5 cm (COZ) which limit the drift time to about 1-2 μs. Both sense wire ends are read out providing a ϕ-measurement via charge division, in addition to the z-position from the drifttime measurement. An accuracy of 250 μm (CIZ) and 340 μm (COZ) is achieved on the z-coordinate.

The z-drift chambers are mechanically linked to the central MWPCs. The part of the CTD which lies closest to the beam contains the inner proportional chamber (CIP) whereas the outer chamber (COP) is situated between COZ and CJC2. Both detectors consist of two layers of multiwire chamber formed by three self-supporting cylinders made of a sandwich of Kapton/Aluminium foils and Rohacell foam. The anode wires are strung along the beam axis. They are not readout. In each chamber, one of the cathodes is divided into rectangular strips (pads) with a regular segmentation in ϕ and z. The readout of the charges induced on these strips provides space points which are used to define the direction of the tracks. Both detectors have a charge collection time below the bunch crossing time and provide an independent determination of the bunch crossing at which an event occured.

The construction of the CIP and COP chambers are very similar. The COP detector, developed by the IIHE, is described in the next section. A detailed description of CIP can be found in [13].

1.4.2.3 Forward Tracker

The radial chambers [14] form the core of the FTD. They have been designed to provide an accurate measurement of the track space point ϕ-coordinate as well as an electron identification by means of transition radiation detection. Each chamber consists of 48 wedges with 12 sense wires and segmented cathodes radiating outwards from the beam pipe (see figure 1.8). The cathode potential varies linearly with radius so that the electric drift field is uniform and perpendicular to the wire planes. An array of field-forming electrodes closes the electrostatic field cage on the faces of the chamber. As a result of the radial geometry, the drift cell is smallest near the beam pipe tending to compensate the increase in particle rate. Each sense wire is connected at the inner radius to its partner 105° away in ϕ. At the outer circumference, both wire ends are amplified and recorded by a readout chain. An accuracy of 110-150 μm on the drift distance and a charge division resolution of about 2 cm are achieved.

Electron identification is obtained from the analysis of the ionization energy deposition due to both the charged particle and radiation photons from the radiator immediately upstream. This latter consists of 400 polypropylene foils of 19 μm kept in Xe at an average distance of 230 μm. When a particle crosses the boundaries between the foils and the gas gaps, radiations in the X-ray region is emitted with an intensity proportional to the Lorentz factor $\gamma = E/mc^2$ of the particle [15]. Consequently, electrons and pions of same energy can be distinguished by integrating the charge deposition on the sense wires. At high momentum ($\sim$ 60 GeV/c), a pion contamination of 8% is obtained for 90% electron efficiency. This identification is further enhanced at lower momenta by the multiple sampling over the 12

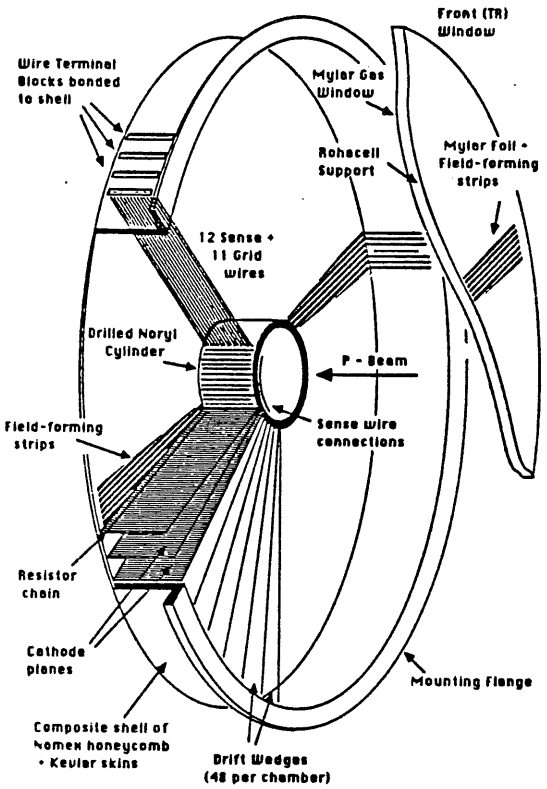


Figure 1.8: Schematic blowup of a radial wire drift chamber

sense wires, resulting at 5 GeV/c in a pion contamination of $\sim 5\%$ [16].

With the radial wire configuration, the polar angle Θ is obtained by charge division with a moderate accuracy. To ensure a Θ resolution of < 1 mrad, planar chambers have been incorporated into the FTD. They also help for the extrapolation of track segments from the radial chambers, especially in certain pathological cases, e.g. particles which fall within the double hit resolution of the radial drift cells. A planar module consists of 3 planes of parallel wires orientated at 60° relative to each other (see figure 1.9). Each of the three planes has a depth of 4 sense wires and consists of a set of drift cells which are rectangular in shape. With this geometry, the spatial resolution is homogeneous in x and y, hence giving accurate measurement of Θ. Furthermore, particles which fall within the double hit resolution of one plane are resolved by subsequent planes with a rotated orientation.

Each forward tracker supermodule contains a multiwire proportional chamber consisting of two adjacent wire planes transverse to the beam and interleaved with 3 cathode planes. The sensitive region is from r = 165 mm to r = 750 mm and covers the full 2π in ϕ. This leads to an angular acceptance of $6.5° < \Theta < 18°$.

A wire plane is made of gold plated tungsten wires with a 20 μm diameter

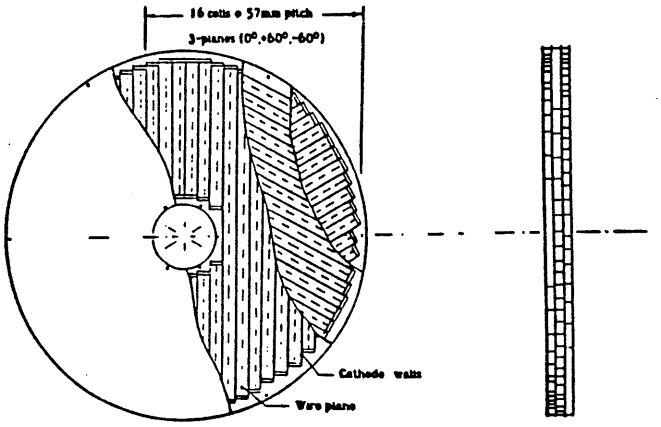


Figure 1.9: Planar drift chambers of the FTD

and spaced every 2 mm. The cathodes are supported on a rigid frame to ensure the flatness and a constant gap of 4 mm between the wire and cathode planes. They consist of a mylar foil, coated with a resistive graphite paint on the side adjacent to the wire plane, and attached to a epoxy board with Cu pads (see figure 1.10). These pads have a ring shape with a segmentation in r and ϕ as

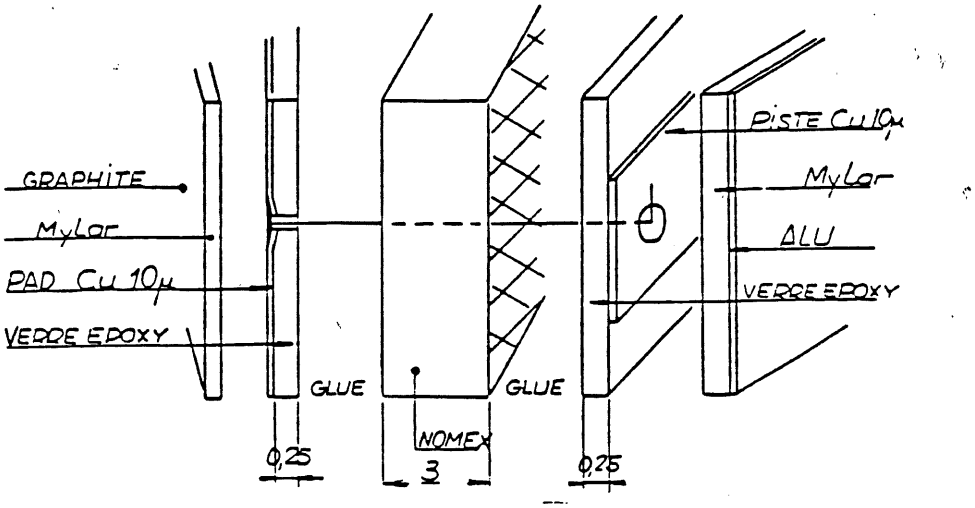


Figure 1.10: View of the cathodes of the forward MWPC

shown in figure 1.11. There are 192 pads on each cathode leading to 1152 channels for the 6 MWPC layers. The pads of two adjacent chambers are staggered in r and ϕ so that the logical granularity is 4 times the physical granularity. They are read out via wires connected through a 2 mm rigid nomex foil and microstrip lines, edged on a fiber-glass epoxy board, to the preamplifiers. An aluminised

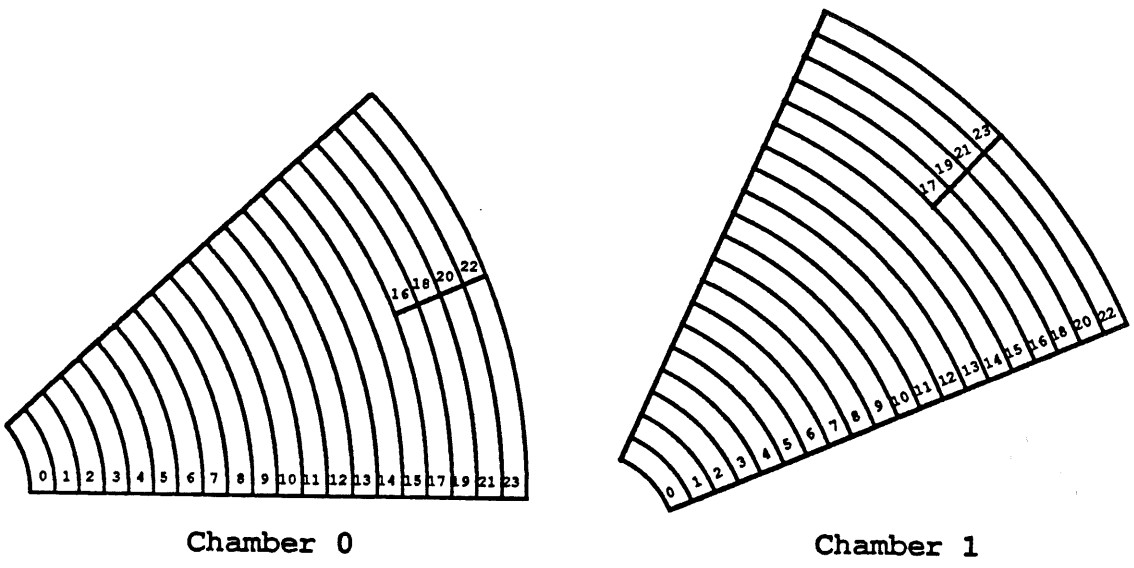


Figure 1.11: Arrangement of pads in the forward MWPC

mylar foil connected to ground is stretched behind the cathode planes to provide an electromagnetic shielding.

1.4.2.4 Backward MWPC

The backward MWPC (BPC) is inserted between the central tracker and the BEMC. Its sensitive region is from z = -1393 cm to z = -1425 cm and r = 15 to 65 cm. It covers the angular range $155^\circ < \Theta < 175^\circ$. The chamber is made of 4 anode wire planes transverse to the beam and oriented at 45° relative to each other. The wires are stretched with a spacing of 2.5 mm between two G10 fiber-glass epoxy rings which ensure a gap distance of 4 mm. Each chamber is closed by two circular G10 plates which provide the mechanical stability and the gas tightness. Only the wires are readout with two wires connected to one preamplifier, resulting in an angular resolution of ~1.0 mrad.

1.4.3 The Outer Proportional Chambers (COP)

The design of the COP detector has been governed by the limited clearance (35 mm) available between the COZ and CJC2 detectors and by the requirement to reduce to a minimum the amount of material around the interaction region. The detector has an active length of 2172 mm with the inner wire plane at a radius of 501.5 mm and the outer at 514.5 mm, corresponding to an angular acceptance of $25^\circ < \Theta < 165^\circ$. The other salient parameters of COP are summarized in

table 1.3.

COP parameters	*Inner chamber*	*Outer chamber*	*Unit*
Total length	2 361		mm
Sensitive length	2 172		mm
Radius of anode plane	501.5	514.5	mm
Anode - cathode gap	4		mm
Anode plane :			
number of wires	1 575	1 616	
wire spacing	2		mm
wire diameter	20		μm
Cathode pads :			
number of ϕ-segments	16		
number of z-segments	18		
Size	12×20		cm^2

Table 1.3: Dimensions and other specification of COP.

The COP chambers are made of three concentric kapton[1] / rohacell[2]/aluminium sandwich cylinders which have been assembled on steel mandrels (see figure 1.12). The inner most cylinder is made of a 4 mm thick rohacell sheet, laminated on both sides with 25 μm thick aluminium foils. The inner Al foil provides an electromagnetic shielding against external perturbation whereas the outer serves as the inner cathode of the first chamber.

The middle cylinder forms the readout cathode of the inner chamber and supports the second detection layer. The readout cathode is made of a kapton foil, 25 μm thick, coated with a resistive graphite paint (200 k$\Omega/\Box$) on the side adjacent to the inner wire plane. The outer surface is glued to a second kapton foil carrying the readout pads. These latter consist of 12×20 cm^2 strips edged on a 1 μm copper layer evaporated on the kapton, and oriented perpendicular to the cylinder axis. In total, the cathode is divided into 16 azimuthal and 18 longitudinal sectors.

The 288 pads are connected with 50 μm diameter copper wires, of up to 2100 mm long, to readout printed circuit boards mounted on the end structure of the chamber. These readout wires are connected to the pads with conductive glue through a 3 mm rohacell layer which carries the wires into grooves cut on its outer surface. A Cu-coated kapton foil, glued on the rohacell, completes the readout cathode. Together with the copper wires, the foil forms a wave guide

[1] Kapton is a polyimide film.

[2] Rohacell is a rigid foam of polymethacrylimide.

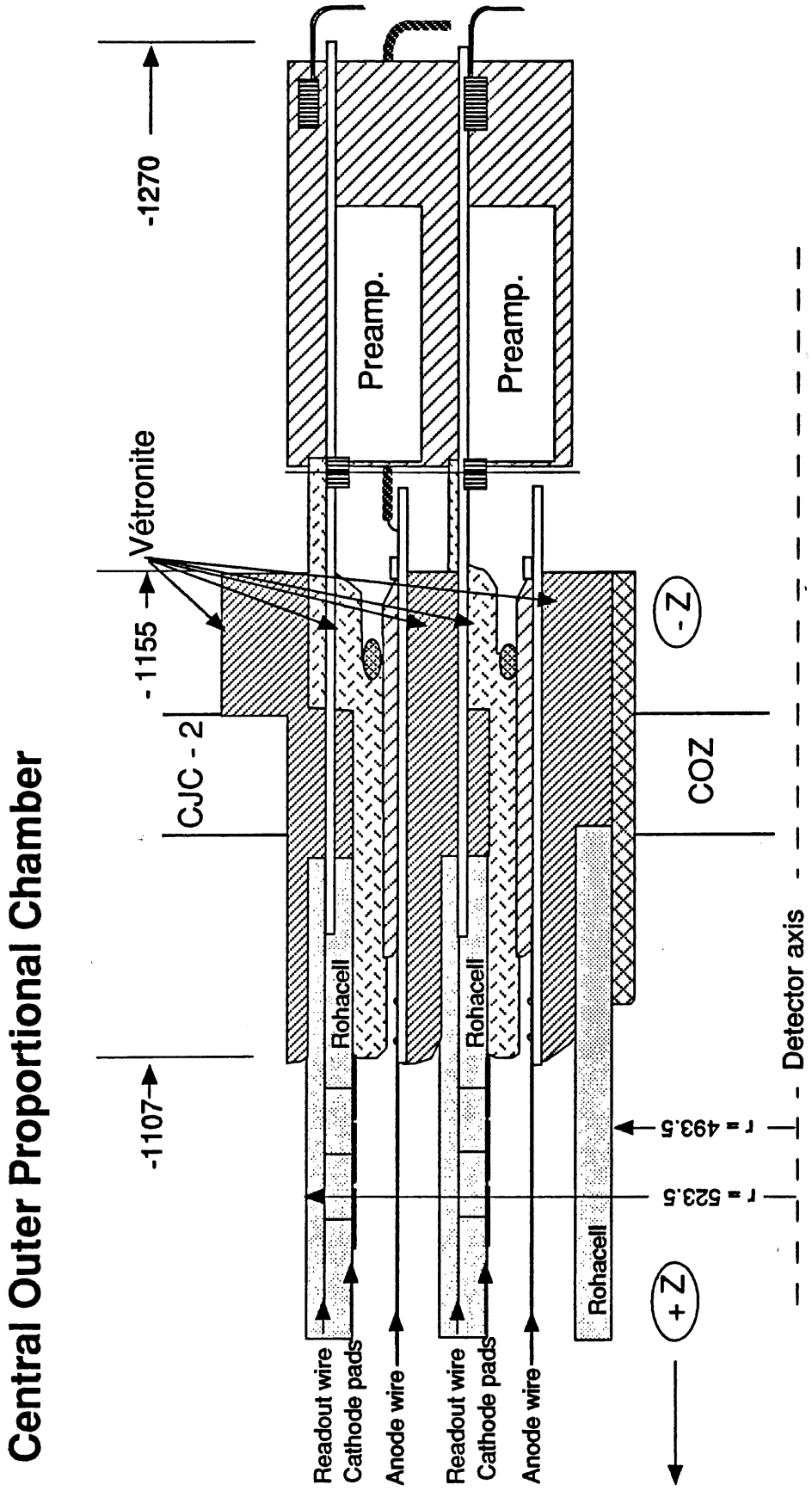


Figure 1.12: Cross section of the COP end structure.

for the signal with a characteristic impedance matched to the input stage of the preamplifier. The middle cylinder is completed by the inner cathode of the outer chamber made of a 2 mm thick rohacell layer laminated with an aluminium foil on the external surface. The stucture of the outer most cylinder is similar to this.

The three cylinders are supported at both ends by glass-fiber epoxy rings which ensure a 8 mm chamber gap height and the gas tightness. Intermediate flanges support the PCBs on which the anode wires and the high voltage connections are soldered. The 20 μm gold plated tungsten anode wires are strung parallel to the chamber axis with a tension of 60 g and a spacing of 2 mm. To ensure electrostatic stability, the wires are supported by two spacers. The flanges on the -z side also support the readout electronics and the gas distribution system.

The chamber operates with a gas mixture of 49.9% Ar + 49.9% C_2H_6 + 0.2% Freon. Using this gas, a high voltage plateau ranging from 2.9 to 3.05 kV is obtained (see figure 1.13). At 3.0 kV, a charge collection time of $\leq$ 60 ns has been measured which allows to use the COP detector for t_0 determination (see figure 1.14).

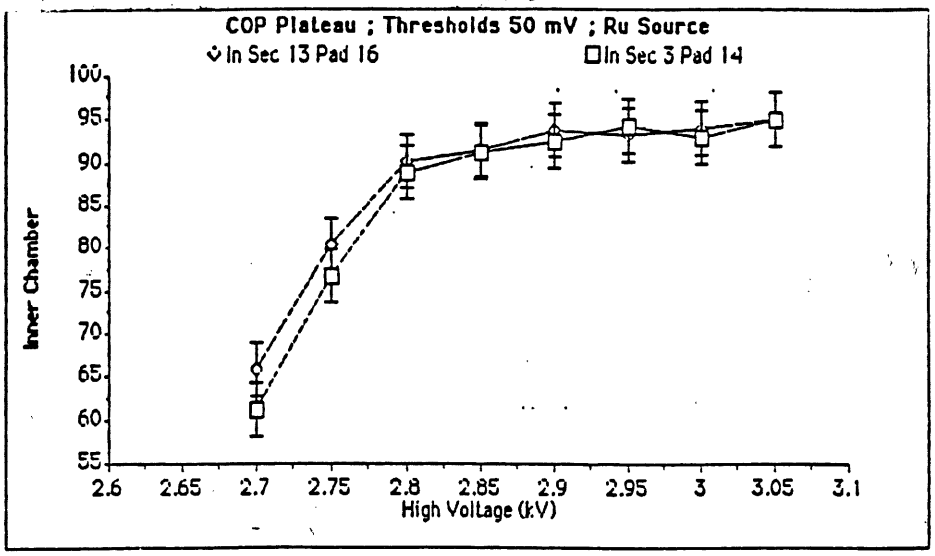


Figure 1.13: COP HV plateau curve.

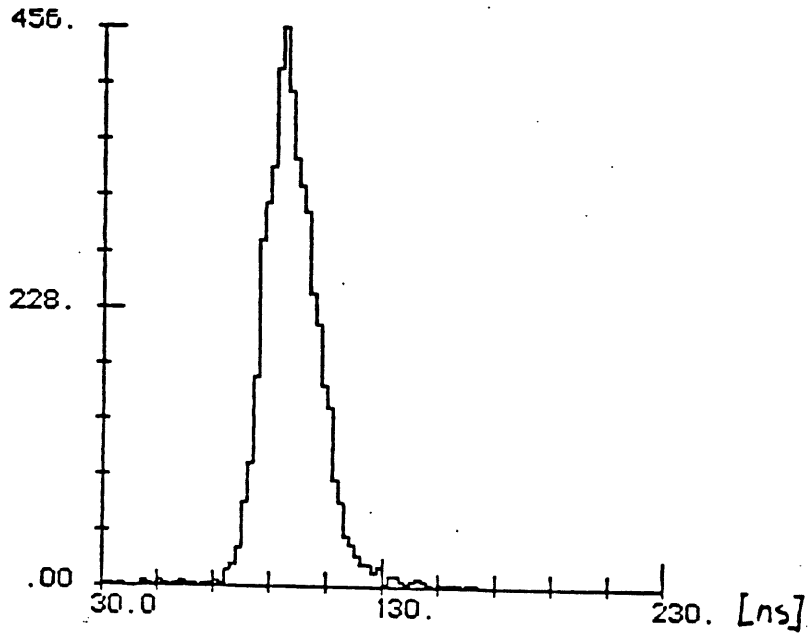


Figure 1.14: Time resolution measured with the COP detector

Chapter 2

The H1 Data Acquisition System

2.1 Introduction

The current high energy physics environment is characterized by the exploitation of relatively high luminosity ($\sim 10^{30} - 10^{32}\ cm^{-2}s^{-1}$) colliders surrounded at the interaction points by large size general purpose detectors. The latter are designed to include a complex arrangement of detector components which cover, as closely as is practicable, the complete solid angle. To permit a precise reconstruction of the physics processes that occur during the collisions, the signals from the detectors must be amplified, eventually shaped, and digitised to extract the desired information, such as the pulse amplitude. This information must then be processed to suppress uninteresting data, to apply calibration corrections, and to format the data to comply with the off-line data structure conventions. The data volumes thus generated are finally assembled and recorded on high capacity storage devices, such as disks and cartridge tapes, for subsequent off-line analysis.

One of the characteristics of large experiments is the utilisation of many types of detectors (calorimeter, drift chambers ...). Each has specific properties and requires a particular approach for signal processing. Consequently, each sub-detector is connected at the bottom of the readout chain to dedicated analogue and digital "front-end" electronics, specially designed to process the signals from this apparatus. The data blocks formatted by the different front-end systems are collected centrally by the "Central Data Acquisition (CDAQ)" system which is responsible for coordinating the overall readout chain and for transferring the full event records to the data store. To maximise the effective use of the experiment run time, these two consecutive readout layers, front-end and CDAQ, must operate under minimum dead time conditions.

The complexity of the detectors and their associated electronic systems require a continuous monitoring of the quality of the data being recorded. For this purpose,

various monitoring systems are connected along the readout chain. Their function is to check regularly the apparatus performance and to detect possible faults in the readout procedure by continuously analysing data samples on-line. As this level, a major concern is the human interface. Facilities, such as event and histogram displays, interactive menus, must be provided to allow any user to monitor the operation of the apparatus and check the running conditions.

In addition to the event processing related tasks, other important functions for the management of the experiment are assigned to the data acquisition system : the setting-up, calibration and test procedures, the control and recording of the critical detector parameters (high voltages, gas flows, temperatures ...), the communication with the off-site systems etc ...

This chapter gives an overview of the H1 data acquisition system and describes the general structure of the system hardware. In section 2.2, we review the environment which has conditioned the readout architecture. The trigger system is described in section 2.3. Sections 2.4 and 2.5 present in more detail the data acquisition system : the consecutive steps of the acquisition procedure and the description of its hardware implementation.

2.2 Basic Design Features

The design of a data acquisition system for a general purpose detector at HERA poses a technical challenge that has no precedent in high energy physics. The high bunch crossing rate (10^7 Hz), the background environment and the scale of the detectors ($>$ 250000 channels in H1) have serious implications on both the hardware and software needed for the event processing. Many aspects of the HERA environment prefigure the situation to be expected at the future large hadron colliders SSC and LHC. In order to stress the extent of the problem, an overview of the principal parameters relevant for the data acquisition is given below.

2.2.1 Bunch Crossing Rate

The most constraining parameter for data acquisition at HERA is certainly the very short bunch separation time of 96 ns. All the detector signals have to be sampled at the frequency of 10.4 MHz, or at a higher harmonic, in strict synchronism with the bunch crossings. This requires a precise timing system broadcasting a synchronization clock (called HCk later), with a nanosecond accuracy, to the front-end electronics distributed around the apparatus. Delays in the front-end electronics need to be carefully adjusted to avoid signal dephasing. Futhermore,

as the detector response times and the propagation delays are often longer than 96 ns, techniques to properly identify the event occurrence time t_0 must be devised.

2.2.2 Event and Background Rates

Event rates may be calculated from the estimated cross-sections of the e-p neutral current and charge current interactions at the centre-of-mass energy $\sqrt{s} = 314$ GeV. A summary of these rates is given in table 2.1. The dominant physics process is the low $Q^2 (Q^2 \sim 0)$ photon exchange, or photoproduction process, with a rate of $\sim$ 1 kHz at the design luminosity. A large fraction of these events produces particles inside the beam pipe so that the visible interaction rate in the detector is $\sim$ 200 Hz. It dominates all the other physics processes : the expected rate of NC events, for $Q^2 > 3\ GeV^2$, is 3 Hz and that of CC events is 10^{-3} Hz. As these rates are very small compared to the beam crossing frequency (10^7 Hz), the probability of multiple interactions in one beam crossing is expected to be negligible.

Source	*Event/s*
Neutral currents:	
$Q^2 > 3\ GeV^2$	3
$Q^2 > 5\ 000\ GeV^2$	10^{-4}
Charged currents :	
all Q^2	$3\ 10^{-3}$
$Q^2 > 5\ 000\ GeV^2$	$5\ 10^{-4}$
Photoproduction :	
all events	10^3
visible in the detector	200
Background :	
halo particles	10^4
beam-gas interaction/m	300

Table 2.1: Expected event and background rates assuming L = $1.5\ 10^{31} cm^{-2} s^{-1}$

The highest rates of particle activity in the detector are expected to come from the background induced by the beams. The proton beam is accompanied by a halo of off-momentum protons ($\sim 3\ 10^4 s^{-1} m^{-1}$) and showers of secondary particles produced by the interactions of the protons with the residual gas in the beam pipe. The electron beam produces also a large amount of synchrotron radiation ($8\ 10^{17} \gamma/s$ with $k > 20\ keV$) due to the bending of the beam close to the interaction region. In addition, cosmic rays during the e-p interaction are non negligible because of the frequent beam crossings. The rate of cosmic muons

passing through the calorimeter is 3 kHz. However less than 0.1 % point to the interaction vertex region. In addition a threshold cut on the cluster energy detected in the calorimeter will reduce the rate to less than 1 Hz.

A large percentage of the background particles produced by the machine is stopped by a complex set of collimators, shielding walls and X-ray absorbers. The particles that still penetrate the detector are essentially concentrated in a narrow cone around the beam axis. Particularly, the tracking detectors and the forward calorimeter see a high rate of low momentum particles from beam-gas interactions produced mainly within 5 m of the crossing region. All this, results in a background rate of about 10^1 Hz in the detector. Thus an overwhelming majority of the particle activity seen by the detector components are background events rather than genuine ep interactions. Consequently, event selection methods have to be devised to discriminate on-line the small number of potentially interesting events against the background.

2.2.3 Detector and Front-End Electronics

The H1 detector is an assembly of embedded detector components which correspond to about 270 000 electronic channels. Table 2.2 summarizes this partition and the amount of data produced by each subsystem. To extract from the diffe-

Components	*No of channels*	*Raw data size*	*Average formatted size (kbytes)*[1]
Drift chambers	9 648	~ 2.5 Mbytes	15
MWPCs	3 936	~ 6 kbytes	2.5
LAr calorimeter	45 000	95 kbytes	13
Calorimeter trigger	50 000	110 kbytes	1
BEMC	1 500	~ 7.5 kbytes	2
Plug calorimeter	800	~ 4 kbytes	1
Muon streamer chamber	160 000	10 kbytes	0.5
Luminosity	256	48 kbytes	1
Total H1	~ 270 000	~ 2.9 Mbytes	36

1. These numbers correspond to the summer 92 runs. At that time, the machine was filled with only 10 bunches and L $\simeq$ 10^{29} cm^{-2} s^{-1}

Table 2.2: H1 components and data partition

rent sensors, the desired and pertinent quantities related to the passage of particles within the detector, e.g. nature and energy of the particles, the signal processing

needs to be adapted to the specificity of each detector element. To illustrate this, let us consider a few examples :

- The determination of the particle energy from the calorimeter signals requires the measurement of charges deposited on readout pads. Charge-sensitive analog-to-digital converters (ADCs) are used for this purpose. As in LAr calorimeter the charge collection time is around 500 ns, the integration time has to be at least of this size to accumulate all deposited charge.
- Time and charge information must be extracted from the tracking chamber signals. For this, the pulse shape has to be recorded in order to allow further numeric processing such as peak finding and charge integration. This recording scheme requires the use of voltage-sensitive ADCs capable of a high sampling rate ($\sim$ 100 MHz) in order to give an adequate representation of 100 ns wide pulses.
- The MWPCs provide space points used for the determination of the beam crossing time and for fast vertex reconstruction. For these applications, the shape of the signal is irrelevant and simple pulse discrimination is sufficient.

After the digitisation of the analog signals, the averaged raw data size per event reaches 3 Mbytes. It is largely due to the use of time-sliced ADCs for the digitisation of the drift chamber signals. To reduce this size to values between 50 and 100 kbytes, data compression and formatting must be performed in situ at the level of the digitising electronics.

2.2.4 Consequences

The considerations briefly outlined above shape the conceptual layout of the signal processing system by imposing some basic conditions to be satisfied :

- To reject a maximum amount of background data before tape recording, trigger decisions have to be taken at various levels, starting with fast and crude selections and evolving to finer filtering when all information for an event is collected. Each level, by reducing the rate of event candidates, affords the subsequent level more processing time.
- Due to the bunch crossing rate, the first level of the trigger system has to provide a decision every 96 ns. As a time of about 2μs is required to get the signals from the detectors and to combine them in the trigger processors, the latter must be able to independently process data from neighbouring beam crossings.

- Data flows through the readout chain and the trigger processors are kept as independant as possible. The signals from the detectors participating in the first decision levels are distributed into a "DAQ" and a "trigger" branch. In the DAQ branch, a hierarchy of local buffers in which events can accumulate until rejected or accepted by a higher level trigger logic is essential to accommodate the trigger latencies.

- To reduce the event size and structure the data for the off-line analysis, on-line preprocessing is mandatory. This is done preferably in the front-end stages of the readout chain to minimise the transfer of large raw data blocks. By combining the raw event size with the digitisation rate (200 Hz), a global bandwidth of the order of 6 10^8 bytes/s is required at the input of the processing chain. Data formatting and trigger rejection must reduce this value to $\sim$ 5 10^5 bytes/s at the data logging level.

The above mentionned conditions require that the data acquisition has to be founded on a distributed multi-processing system providing a high degree of parallelism for the handling of the data. Its architecture will be based on a tree structure, with separate branches at the level of the front-end electronics and processor farms where full-event building and filtering are performed.

2.3 Overview of the H1 Trigger System

2.3.1 Introduction

The task of the trigger system is to select the potentially interesting events, i.e. charged and neutral current interactions, as well as possible exotic physics processes, and to reject the particle activity associated with the background sources. This selection is made by combining information from the various detector components and by looking for properties of distinctive final state, e.g. high energy electron, missing energy. Because of the extremely high rate of complex background events and the unprecedented beam crossing frequency, the design of a trigger system at HERA is a challenge. Trigger decisions have to be taken in very short times with a high degree of selectivity and sensitivity power.

The H1 trigger system [17] works in 4 levels, designated by L1...L4 which are progressively more complex and more time-consuming (see figure 2.1). Each level Ln decides between keeping or rejecting an event. In the latter case, the event is eliminated without any possibility of recovery. If the event is accepted, it is submitted to the next selection level Ln+1, applying more restrictive criteria, and the associated data are moved further in the readout chain. The events which survive to L4 are recorded on cartridges. The two first levels, L1 and L2, are

specialized hardware processors with a fixed latency, while the levels L3 and L4 are based on RISC farms. In the following sections, we give a more detailed overview of the event selection procedure. Next, the synchronization of the readout data flow with the trigger levels is described.

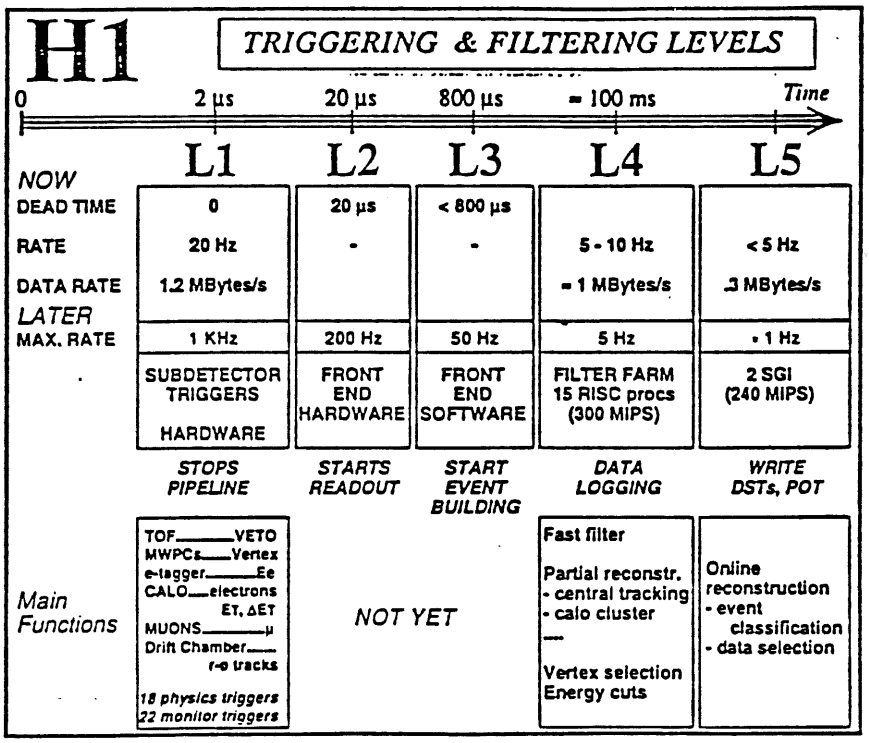


Figure 2.1: Triggering and filtering levels

2.3.2 Level 1

The first level trigger selects the initial candidates for data processing. It has to evaluate the data from each bunch crossing and therefore provide a decision every 96 ns. For most detector components, this time is too short to get the signals and make logical combination. Therefore, the first trigger decision is postponed until 2.1 μs after the crossing. Consequently, in order to have a dead time less first level the trigger logic must be able to process independently data from neighbouring beam crossings. For this purpose, a "pipelined" triggering system has been developed. Figure 2.2 illustrates its basic concept [18]. The signals of the detector are first synchronized with the bunch crossing frequency and then sent into the decision logic. The data processing is subdivided into n consecutive steps, each one taking less than 96 ns. On every clock cycle, the output data of each stage are shifted forward through the pipeline. At the same time, a new decision appears at the output of level 1 uniquely related to a single bunch crossing which occured n

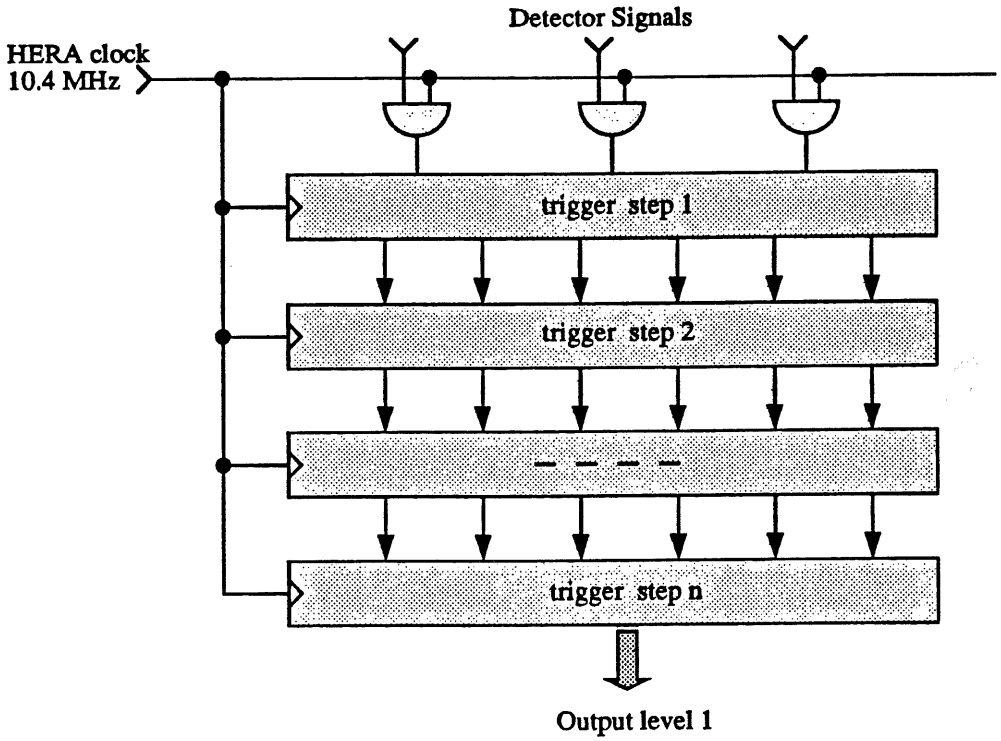


Figure 2.2: Pipelined trigger for the decision level 1.

clock cycles before. If the decision is positive (L1keep), the L1 processor stops and the event is submitted to the L2 logic. In this way, although the total L1 decision time is much larger than 96 ns, no dead time is generated until a L1keep decision is made. As the L2 decision time is 20 μs, the L1keep rate should be at most 1 kHz to limit the dead time introduced at the second level to a few percent[1].

The data used to form the L1 decision come from various detector components: calorimeter, central tracking, MWPCs, muon detection system and the scintillator counters. These detectors provide local trigger elements, based for example on the transverse energy deposited, the missing energy or the track multiplicity found in restricted regions of polar angle. They are centrally combined in the L1 Central Trigger Logic (CTL1). The MWPCs provide two sets of such elements based on a "Z-vertex" and a "Forward ray" logics:

- The Z-vertex trigger [19] provides a fast reconstruction of the vertex position along the beam axis. Its purpose is essentially to reject background from beam-gas or beam-wall events outside the e-p interaction region. The trigger logic searches all the possible combination of four hits in the central MWPC chambers (CIP, COP) and the first forward MWPC pair which can

[1] At the time of writing, only the level 1 and 4 were operational with an output rate of $\sim$ 20 Hz and 5 Hz respectively at $L \simeq 10^{29} cm^{-2} s^{-1}$.

be connected by a straight line in the r-z plane. The intercept in z with the beam axis of the ray candidates is entered into a histogram, in which the whole interaction region is divided in 16 bins of ~ 5 cm width (see figure 2.3). Combinations of hits not belonging to the same particle track produce a flat distribution in the histogram, whereas a significant peak is found at the true vertex location. Background events produced outside the interaction zone do not produce a peak in the histogrammed region and can therefore be rejected by a cut on the peak significance. Figure 2.4 illustrates the results obtained with real deep inelastic and background events.

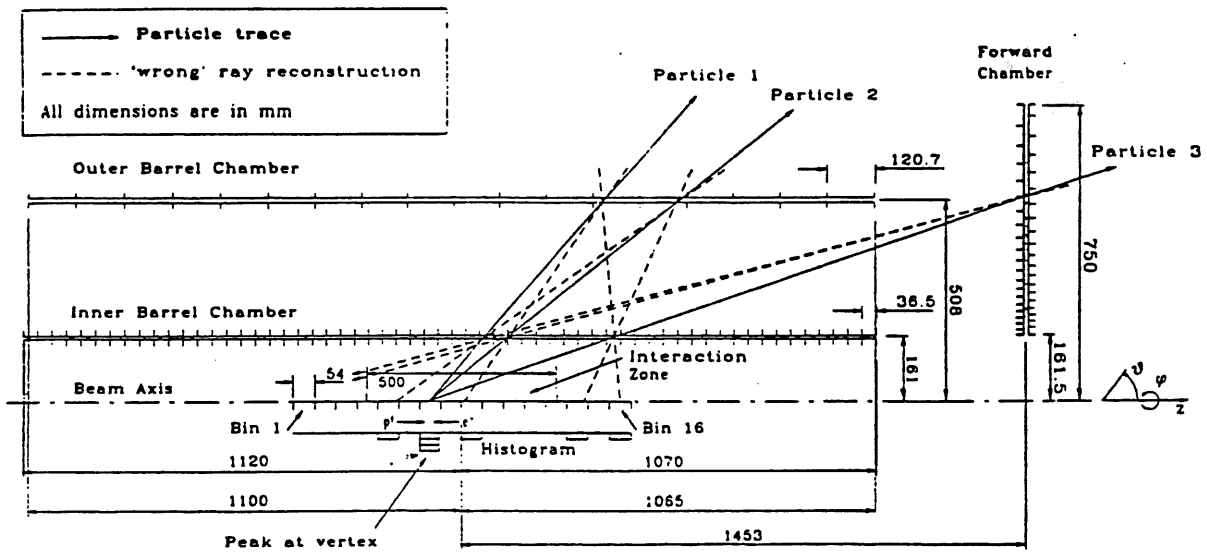


Figure 2.3: Z-vertex reconstruction using the MWPC pad signals

- The forward ray trigger [20] identifies the tracks of charged particles coming from the interaction region in the forward direction. The information from the 3 pairs of forward MWPCs and from the forward part of the inner barrel chamber (CIP) are combined to define the track candidates. A coincidence of at least 5 hits in the low and high Θ-regions, and of 7 hits in the medium Θ range, pointing to the interaction region, is required to form a ray. The pad segmentation allows to define 32 rays for each of the 16 ϕ-sectors. The decision is based on the ray multiplicity.

The MWPC triggers are used to tighten up on calorimeter triggers. To achieve this, coincidences between the MWPC rays and the corresponding calorimeter signals are made. This allows to set lower energy thresholds, without summing to much noise, and extends the possibility to trigger on events with not much energy deposited in the calorimeter, e.g. low Q^2 charged or neutral current events.

The trigger elements generated by the different detector components are com-

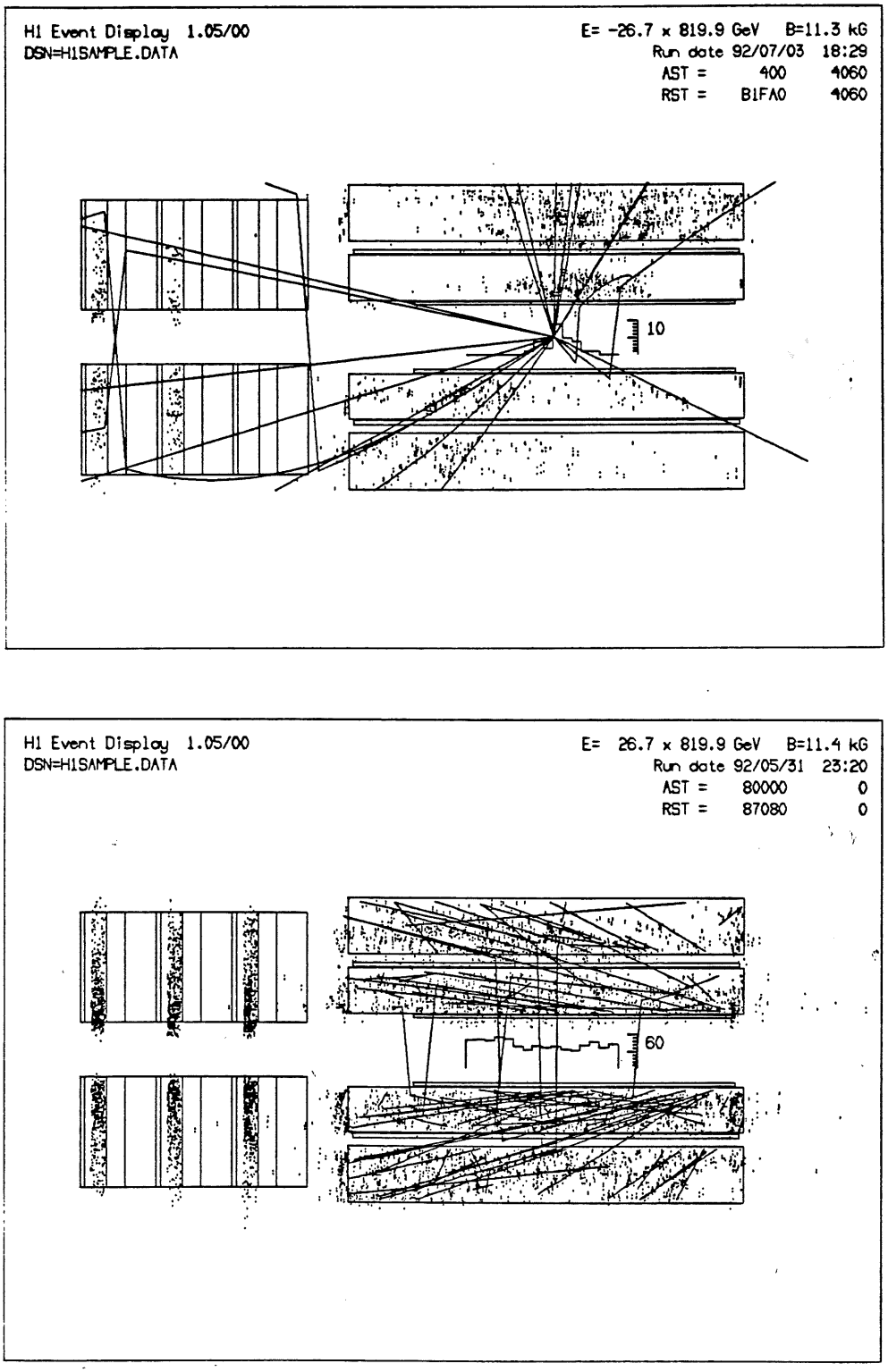


Figure 2.4: Z-vertex histograms for a) a typical deep inelastic event and b) beam-gas background outside the interaction region

bined in the Central Decider of the CTL1 system [21]. Figure 2.5 shows a schematic overview of its logic. The digital signals supplied by the subsystems are first syn-

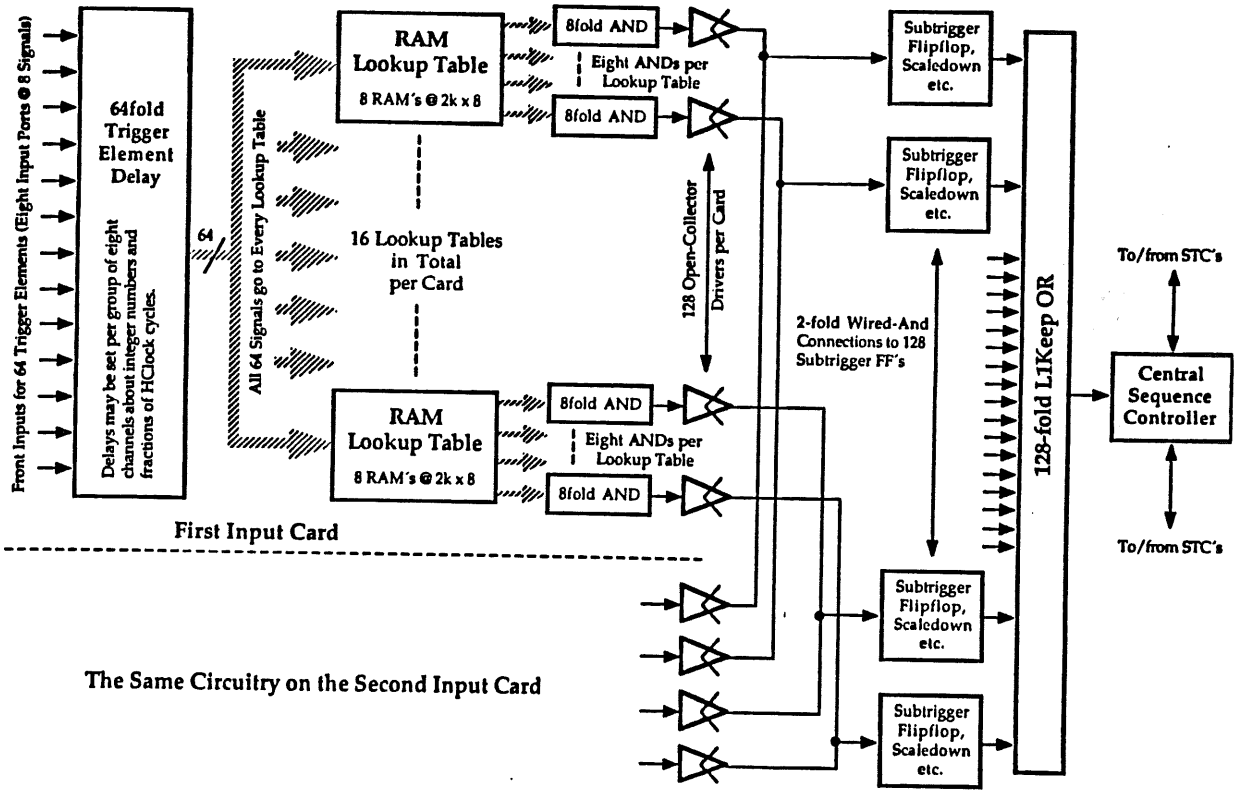


Figure 2.5: Schematic overview of the L1 Central Trigger Decider

chronized by means of programmable delay units. This ensures that all information related to the same bunch crossing is presented to the subsequent logics during the same clock phase. The delayed signals are driven to the address inputs of a RAM array containing lookup tables. These memories are loaded with bit patterns describing the results of logical operations applied on any combination of the trigger elements. In this way, specific input patterns may be selected to give triggers of a general nature indicating significant particle activity in the detector, as well as more specific signals for high-p_t leptons or large missing E_t.

The outputs of the tables drive a wired-AND logic to form the subtrigger conditions. As an example, the Z-vertex elements are used, together with the TOF and VETO scintillator signals, as a strobe to veto on background events. The status of these signals is latched into 128 flip-flop circuits which are OR-ed to form the L1 decision.

2.3.3 Level 2

The time restriction of 2.1 μs for the L1 decision allows to exploit only partly the information from the detector components. At the level 2, 20 μs are available and the track search in the drift chambers can be made with the full sense wire information. A five times finer granularity on the reconstructed tracks in the CJC is obtained. An additional rejection factor is expected to be gained from topological selections based on the analysis of the energy flow in the calorimeter. Solutions using neural networks are presently being prepared [22]. After this level, the rate of event candidates should be reduced to less than 200 Hz.

2.3.4 Level 3

A positive decision of the L2 trigger starts the digitisation and the readout of the detector information. This increases the dead time by at least 0.8 ms, the time needed to digitise the calorimeter signals. The third trigger level has the function to save on this time by rejecting a substantial majority of the L2 triggers well ahead of 0.8 ms. This will be done by sharpening the cuts made in the previous stages on the basis of calculation in reduced instruction set microprocessors (AMD 29K RISC). If an event candidate is found to be uninteresting before 0.8 ms, the readout process is aborted and the dead time ends after the restart cycle. On the other hand, in the case of a L3keep or no response of the L3 processors before 0.8 ms, the event is kept for further filtering.

2.3.5 Level 4

After the L3 trigger, the event rate is reduced to about 50 Hz. Even after this drastic rejection, background data still dominate the true e-p interaction sample. Further on-line filtering is therefore mandatory for maximising the good over background event ratio. In addition one selects candidates of rare processes for immediate off-line analysis. The filter configuration which has been favoured in H1 consists of a battery of RISC processors embedded in the data acquisition system. This processor farm executes on-line filter algorithms on full event data which are normally run off-line. For instance, the charged particle tracks and the vertex position are reconstructed from the tracker signals, the cosmic muons are filtered out and the energy thresholds of the calorimeter trigger are adjusted with tighten tolerances. The processing time is limited by the real time constraint of about 100 ms per event.

Events selected by the filter are directed to the DESY IBM mainframe to be stored on disks and cartridges. The L4 rejection factor is adjusted such that the

logging rate does not exceed the 5 Hz limit of the storage media.

2.4 Logical Structure of the Data Acquisition Chain

The data flow through the data acquisition chain is schematically represented in figure 2.6. It starts with the readout of the analog signals from the detector and ends with the transfer of the data on magnetic cartridges. To reduce dead time losses to a minimum, a multilevel system with data being buffered where processing latency occurs has been developed. This structure allows the de-randomisation of the consecutive stages of the acquisition procedure so that the performance of the system is determined by the mean trigger rate and event size rather than peak values. This section presents the logical structure of the acquisition procedure. Its hardware implementation is detailed in the next section.

2.4.1 Front-end Signal Storage

The first-level trigger takes 2.1 μs to deliver its decision to the detector front-end electronics. During this time, the information from the detector must be stored for each channel in storage devices. Two different storage architectures are used in H1.

- The signals from the wire chambers are continously digitised by fast discriminators (MWPCs, muon streamer chambers) or by analog-to-digital convertors (tracking and forward muon drift chambers). The encoded data are stored in pipeline memories which accept new information at a rate $f_s = n f_b$, integer multiple of the bunch crossing frequency $f_b = 10.4$ MHz. The MWPC and muon pipelines are clocked at 10.4 MHz, i.e. the signals are integrated over 1 bunch separation time (96 ns), whereas the tracker signals are sampled at $f_s = 104$ MHz. The number of storage elements, i.e. the depth of the memory, has been chosen such that the complete track information of an event may be stored until the L1 decision is taken for this event. They are respectively 32 ($\sim$ 3.1 μs) and 256 ($\sim$ 2.5 μs). Upon a L1keep signal, the feeding of the pipeline is stopped and no further input data is accepted.

- The storage of the calorimeter information is based on an one-stage analog memory. The preamplified analog pulse is continously shaped into a bipolar signal with the peak amplitude at the L1 decision time. The shaper is followed by a sample/hold circuit which tracks the signal when the system is waiting for a L1keep. When a L1 trigger occurs, the S/H switch opens

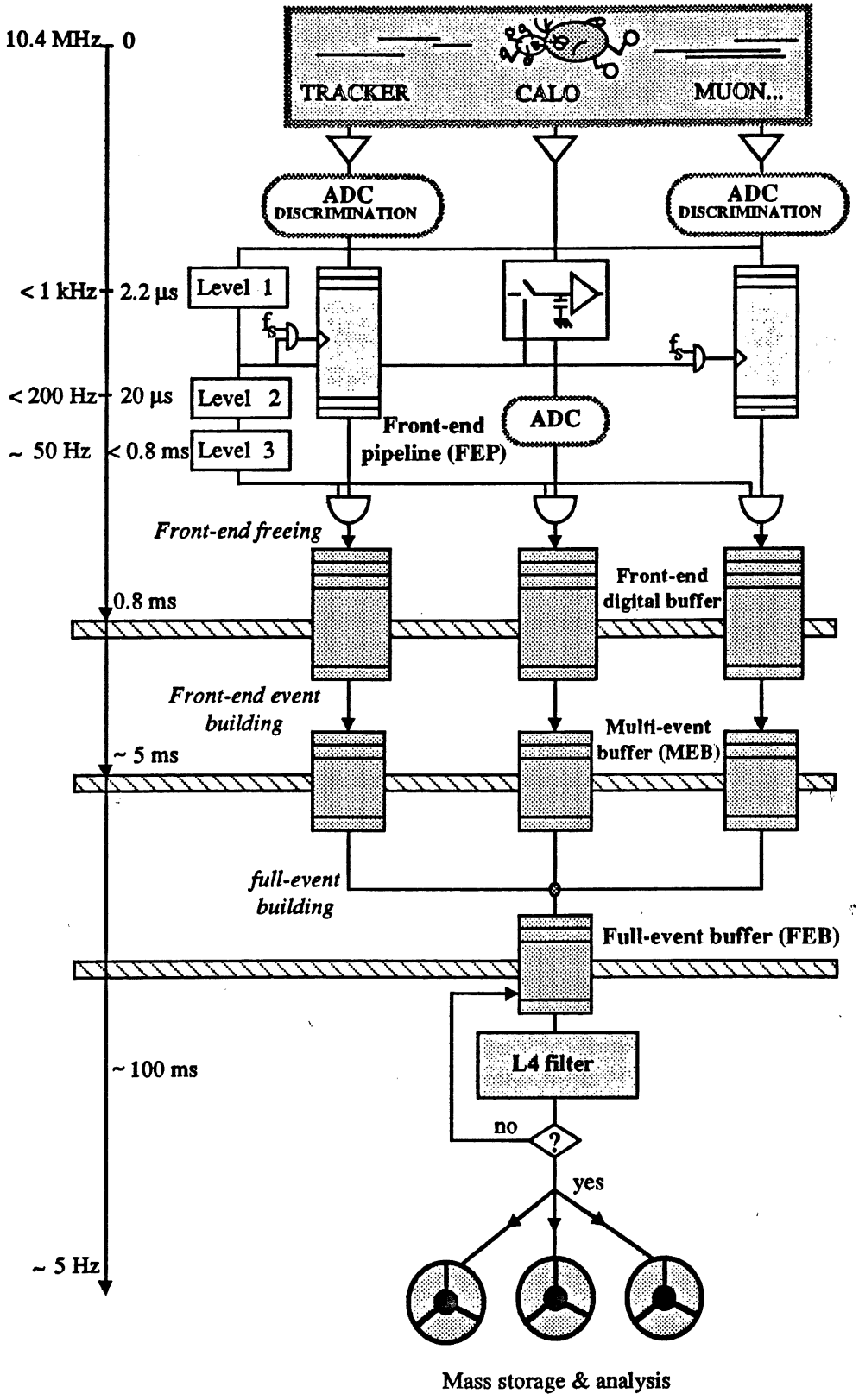


Figure 2.6: Schematic view of the data flow through the acquisition chain

and the storage capacitor holds the voltage between its electrodes until it is closed again on a restart cycle.

Be the storage elements digital or analog, the data acquisition of all the detectors must be carefully synchronized with the bunch crossings. This requires the implementation of synchronization circuits locked on the beam frequency over the whole area of the detector and readout systems.

2.4.2 Front-end Freeing

The second-level trigger decision occurs 20 μs after the interaction. In case of a L2reject, a restart cycle is initiated in the front-end electronics. The data in the pipelines are discarded and the signal sampling is reactivated. If the event is accepted (L2keep), the data from the whole detector are moved into front-end buffer memories. The objectives of this transfer are twofold :

- Free the pipelines rapidly to minimise the detector idle time.
- Buffer locally the data to allow the next stages of the data collection to run asynchronously from the first one.

Since the front-end buffers are digital memories, the voltages stored on the S/H capacitors must be first converted by ADCs. As a very large volume of data is involved, this conversion takes $\sim 0.8\ ms$. During this time no further data taking is possible. To limit the dead time to this value, all other storage devices must be freed before the end of the ADC processing. Once the data have been placed in the front-end buffer, the central trigger controller enables the pipelines again. At that time, the system is ready to accept new events and the first order dead time is over.

In the transfer, some local data preprocessing is performed by custom processors (DSP, scanners) to reduce the event size of the detectors with large amount of data (calorimeter, drift chamber, muon detector). At the same time, the L3 decision is produced. If an event candidate is found to be uninteresting before the end of the transfer, the readout processes are aborted. All the systems then reinitiate the acquisition electronics and wait for a new cycle. This procedure allows to save on the dead time introduced by the front-end freeing by rejecting a fraction of the L2 triggers well ahead of 0.8 ms.

2.4.3 Front-end Event Building

Following the front-end freeing, the data of the event candidate are collected in each branch from the front-end buffers and deposited into a contiguous data block in a Multi-Event Buffer (MEB). This transfer runs asynchronously from the previous stage and therefore generates no dead time, as long as no buffer is saturated. The data are sequentially read from the front-end buffers and assembled into data banks with the appropriate data structure. Further processing is performed to reduce the amount of data, such as zero suppression (MWPC) or charge and drift time determination (DC). This processing is performed by versatile microprocessors embedded in the acquisition electronics and may require several milliseconds for some detectors.

2.4.4 Central Event Building and Mass Storage

The last stage of the on-line data taking is usually referred to as " Central Data Acquisition (CDAQ)". Its main task is to collect from the different multi-event buffers the complete data for each event, merge them into full event records and, after a final filtering, store the output stream on recording media for off-line data analysis.

The final rejection of background events is provided by the L4 filter installed within the main data stream. In this way, the filter has access to the full data, unlike the other trigger logics which work with restricted information. Events selected by the filter are directed to the DESY IBM mainframe to be stored on disks and magnetic tapes. All the events logged on tapes are reconstructed quasi on-line on a Silicon Graphics RISC workstation with 6 processors. An event classification is carried out to select events to be written on production output cartridges and to data summary tapes (DST). These contain all events which are considered to be of interest for the physics analysis.

2.5 Hardware Implementation

2.5.1 Introduction

The hardware organisation of the H1 data acquisition system is based on the natural division of the whole detector into several subcomponents (calorimeter, muon chambers...). The system is composed of the "front-end subsystems", responsible for the analog readout, digitisation and compression of the detector signals, and of the "central data acquisition (CDAQ)", coordinating the full event building and

the data recording, in parallel with filtering and monitoring tasks (see figure 2.7). Data and messages are exchanged between the two layers through the multi-event buffer attached to each branch [23].

The front-end subsystems consists of 12 branches, each one processing the data of a set of detector components or trigger systems. This partition is summarized in the table 2.3.

Branch	*Detector trigger system*
1. Trigger	Central trigger controller (L1 and L2 logics)
2. Calorimeter trigger	LAr trigger system
3. Calorimeter ADC	LAr calo., BEMC, plug and tail catcher readout
4. Central tracker	CJC, CIZ, COZ readout
5. Forward tracker	Planar and radial chambers readout
6. Forward muon	Muon spectrometer readout
7. MWPC	MWPC and associated triggers readout + TOF
8. Muon	Muon streamer chamber readout
9. Luminosity	Luminosity calorimeter readout
10. Forward muon trigger	Muon spectrometer trigger system
11. Subsystem triggers	Central DC trigger systems
12. Test	Only for transfer tests

Table 2.3: Branch partition of the H1 data acquisition system

Each branch is autonomous and can be operated, in addition to the centralised data taking mode, as an independent unit for commissioning and test measurements. Its implementation is obviously strongly influenced by the characteristics of the associated subdetector, e.g. number of channels, signal digitisation technique used, etc... As a consequence, each branch has its own configuration based on specific acquisition modules, interfacing and computer systems. However, the differences lie more in the details and specification of components used rather than with any fundamental design concept. The drift chamber and calorimeter systems are described as examples in the section 2.5.3, while the next chapters are completely devoted to the description of the MWPC front-end readout system which is our contribution to the H1 experiment.

The connection of the front-end branches to the central part of the acquisition chain imposes some degree of standardization at the point where they are merged. So each front-end system has a dedicated readout controller processor which is responsible for the handling of the communication with the CDAQ and for collecting

the data from the front-end buffers into its MEB. To provide a coherently managed system, these components and the communication paths follow the IEEE 1014 VMEbus specification which has been chosen as the H1 bus system standard. As a rule, the crate housing the readout controller and the MEB, often termed as the "subsystem Master Crate", and the CDAQ system are VMEbus based. Most of the front-end systems are also developed in this framework but the use of other busses is not excluded at this level. Since an extensive use of the VMEbus is made, a short introduction to its specification is first given. Next, the hardware implementation of the front-end systems and the CDAQ is described.

2.5.2 The VMEbus

The VMEbus (short for Versa Modules Europe bus) is a modular interfacing system used to interconnect, within a rigid framework, processing, data storage and peripheral control devices. It has been conceived with the objectives to allow high speed communication between electronic modules in a full 32-bit distributed multiprocessor architecture.

Adopted in 1981 by a consortium of firms (Motorola, Philips, Mostek, Thomson) to support the 68000 processor family, VMEbus has been approved as IEC standard 821 in 1986 and IEEE standard 1014 in 1987. It is now supported by hundreds of manufacturers worldwide and consequently has a very large product inventory. The following text provides an introduction to the VMEbus specification and to some extensions which are used in the context of the H1 data acquisition system.

2.5.2.1 General VMEbus Features

A VMEbus system [24] consists of a global bus connection, or "backplane", and a collection of functional modules which communicate with each other using the backplane signal lines (see figure 2.8). The backplane is a multilayer printed circuit board with 96-pin DIN connectors and signal paths that bus the connector pins. It is divided in 2 parts, called J1 and J2. The J1 backplane is the main VMEbus connection and is located in the upper-most position of the card cage. It provides the signal paths needed for operation in 16-bit data and 24-bit address format. The J2 backplane, located below the J1 , completes the 32-bit architecture and allows the extension of the VMEbus to auxiliary busses (e.g. VSB, see below) or I/O connection. In a standard configuration, the backplane may support up to 21 functional modules including processor boards, memories, I/O controllers, etc...

The VMEbus is organized around the concept of master and slave elements. A data transfer cycle is initiated by a master which first establishes the communica-

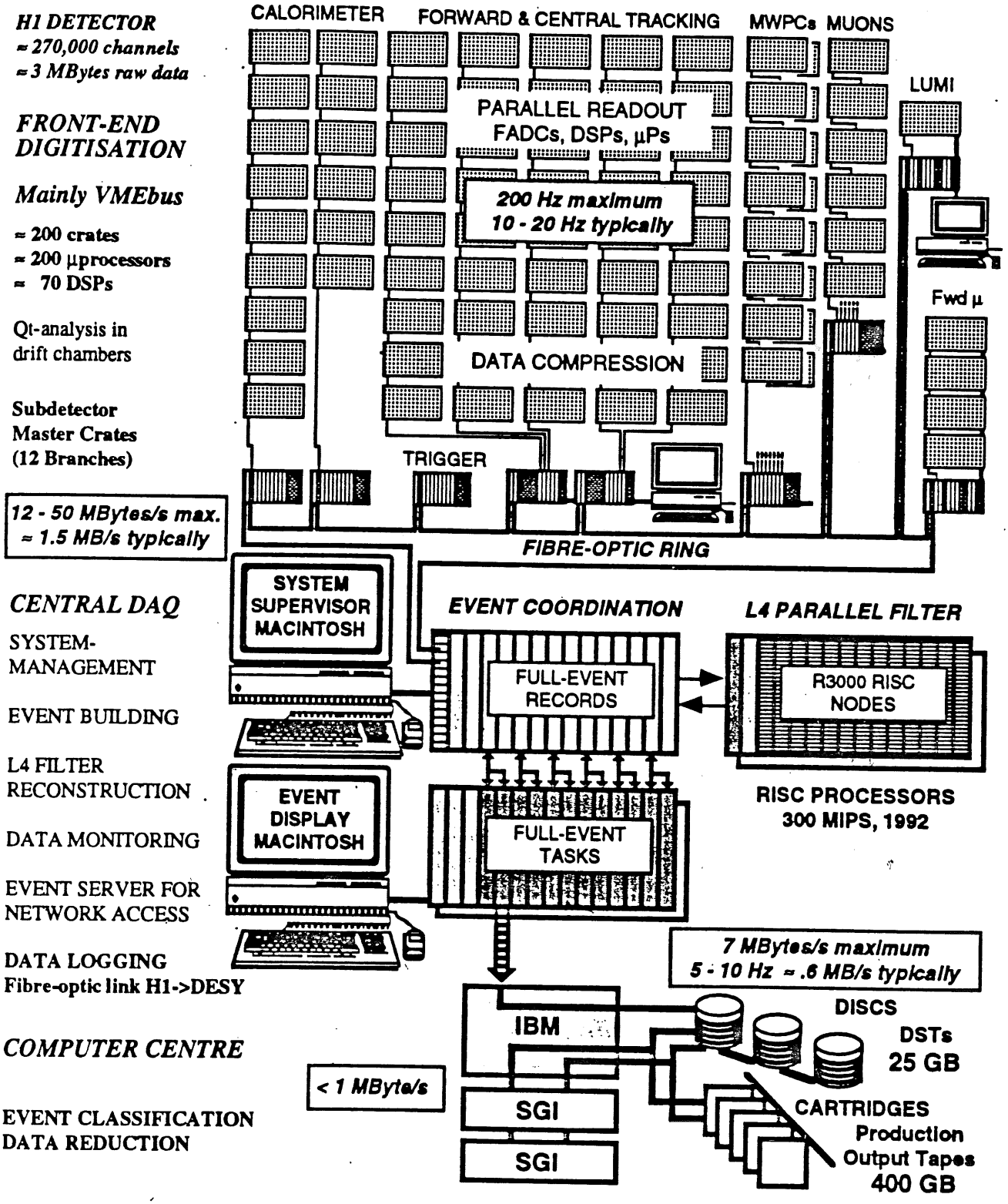


Figure 2.7: Physical layout of the H1 data acquisition system

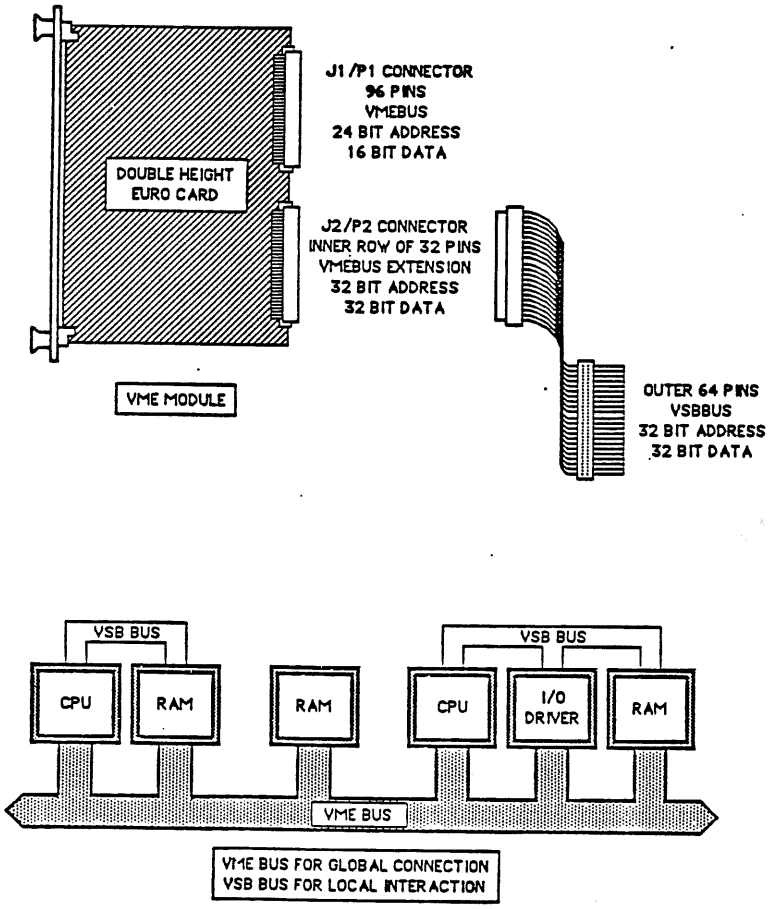


Figure 2.8: VME bus architecture

tion with a slave during an address phase. Afterwards, the binary information is transferred from the master to the slave in a write cycle or in the opposite direction in a read cycle. Four groups of signal lines are provided on the backplane to handle the communication between master and slave modules :

- A data transfer bus (DTB) which contains non-multiplexed data and address dataways and associated control signals. It is used by the master modules to select memory-mapped storage locations on the slave devices, and to transfer data to or from those locations. There are four basic data transfer capabilities, byte (D8), word (D16) and longword (D32) transfers, which allow to interface different type of processors and peripherals to the bus. Direct addressing is allowed in three address ranges : short (A16, 64 Kbytes), standard (A24, 16 Mbytes) and extended (A32, 4 Gbytes). Six address modifier (AM) lines allow the master to pass additional binary information to the slave which may be used, for example, for privileged access or distributed memory management.

  The data transfers on the DTB are asynchronous. After initiating a data transfer cycle, a master waits for a response from a slave. When it detects it, it releases the signal lines and terminates the cycle. This protocol allows the

slave to control the time taken for the transfer so that various processors and devices can operate at different speeds. In addition to the usual single transfer cycle, VMEbus supports also read-modify-write, address-only and block transfers. In this last mode, a maximum bandwidth of about 20 Mbytes/s may be achieved in practice. In the H1 readout system, the addressing possibilities have been extended with the use of the so-called broadcast mode which allows to write simultaneously a data word into several slave modules during a single write cycle.

- A data transfer arbitration bus which allows to coordinate the data transfers when the system supports multiple processors. This bus is controlled by an arbiter module, usually located on a master, that decides which master should be granted control on the DTB when several masters request it at the same time. This prevents simultaneous use of the bus by two masters and to schedule the bus requests for optimum bus use.

- A priority interrupt bus which provides signal lines by which devices can request service from a processor. These requests can be prioritized into a maximum of seven levels with up to 256 vectors.

- An utility bus which provides initialisation and failure detection lines and periodic clocks. It includes a system reset line, system and AC fail lines, a serial data line and two independent clock signals. The backplane carries also power supply lines (+ 5 V, ± 12 V) and ground connections.

Although claimed to be processor-independent, the VMEbus backplane and the associated communication protocol are optimized for 680x0 processors. As a consequence, most of the available VME CPU board products are developed around this processor family. This is particularly the case for the CPU boards used in the H1 data acquisition system which are based on the 68020/68030/68040 microprocessors.

2.5.2.2 The VSBbus

The VMEbus is a global bus, this means that data transfers can take place between any master-slave pair. In a multi-master configuration, the bus bandwidth must therefore be shared between different processors. Problem of bus latency may occur whenever the DTB is loaded to the limit of its bandwidth. Masters using a high priority level and transferring large amounts of data may prevent other boards of seizing the bus and hence degrade the overal system performance. The VME Subsystem Bus (VSB) [25] has been designed to provide a solution to this problem. It allows to transfer part of the traffic from the global bus to parallel local busses connected within the overall framework of the VMEbus system (see figure 2.8). In short, a VSB connection consists of a backplane which occupies the

outer two rows of 64 pins on the lower J2 VME connectors of up to 6 boards. In this way, local computer clusters may be created in which a processor may access private resources without disturbing the activity on the VME. This configuration is actively employed in the H1 readout system to avoid the interference between the different stages of the acquisition procedure.

2.5.2.3 Multi-Crate Systems

High-energy physics experiments require a large amount of crates, nearly 200 in H1, to house the data acquisition electronics. These crates need to be interconnected to transfer data between the different parts of the system. Unfortunately, the VMEbus has been conceived as a single crate system and no formal specification exists for high rate crate-to-crate link. Specification are also missing for connecting VMEbus systems to external control computers. Several solutions have been developed by manufacturers and are presently in use, also within the H1 experiment. They will be presented in the following sections describing their hardware implementation.

2.5.3 Examples of Front-end Electronics

This section is intended as a summary of the techniques used in the front-end systems for digitising and compressing the detector information. The implementation of the two main front-end subsystems, the drift chamber and the calorimeter readout, are described.

2.5.3.1 Drift Chamber Readout

The drift chamber (DC) readout system processes the signals from the 10 000 sense wires of the central drift chambers (CJC, CIZ, COZ), the forward planar and radial modules and the forward muon detector. It represents the largest contribution to the raw event size, producing over 2 Mbytes of information for each triggered event [26].

The determination of the three coordinates of track space points requires the measurement of the drift time and the integration of the charge at both ends of the sense wires. The charge measurement provides also information about the ionization loss and therefore about the particle type. The technique which has been favoured is based on flash ADCs (FADCs) which record the development of the chamber signal in steps of 9.6 ns [27]. The output binary data of the FADC are used to obtain a digitised representation of the signal pulse shape on which numeric processing can be performed, e.g. peak finding, pulse integration and

pile-up unfolding (see figure 2.9). This technique allows precise measurement of

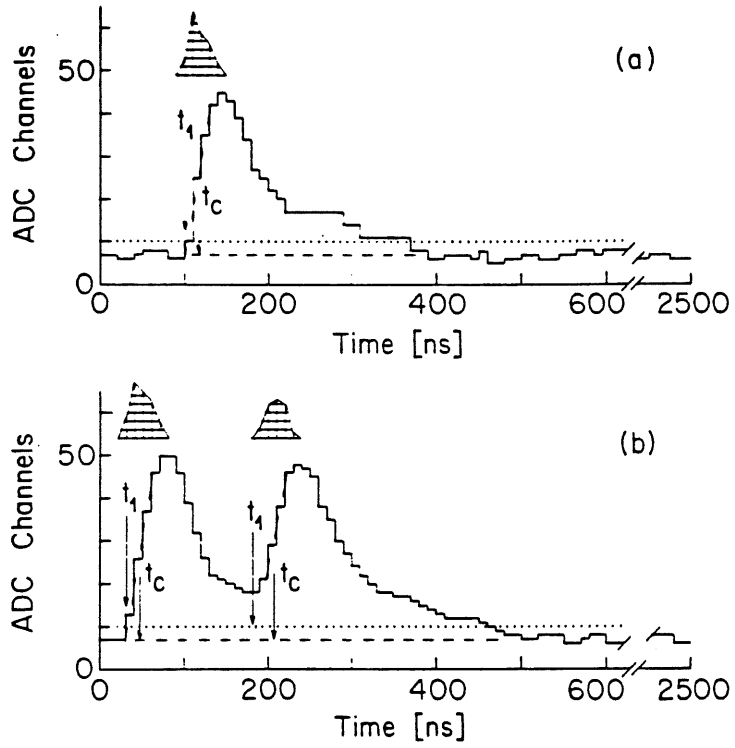


Figure 2.9: Reconstruction of CIZ signals with a FADC (a) is an isolated pulse and (b) is a separable double pulse. The horizontal dashed line is the pedestal and the dotted line is the threshold for pulse detection. Taken from [28]

drift time and signal charge with a much better accuracy than with conventional drift chamber electronics using TDC and charge storage devices. Particularly, the contribution to the spatial resolution of the electron diffusion along the drift path can be reduced substantially if appropriate algorithms are used for the pulse shape analysis. Furthermore, the recognition and the reconstruction of double-hit structures, frequently produced in dense jets, are greatly improved with this method.

The DC acquisition system is housed in 45 triple-height Euro crates based around VMEbus. Each crate is equipped with 16 digitising boards, a fast scanner module, a 68030-based readout processor and a crate interconnect (see figure 2.10). In total, 256 channels are readout in each crate. A digitising channel consists of an 8-bit, non linear, FADC which samples continously the analog signal with a frequency of 104 MHz. The FADC dynamic range is 8 bits to account for the wide range of pulse-heights at different track angles, specially in the central detector. The encoded data of every channel are stored into a 256 byte wrap around memory. On the occurrence of a L1 trigger, the FADC sampling is stopped so that the memory keeps the data associated to the event which caused the trigger. On

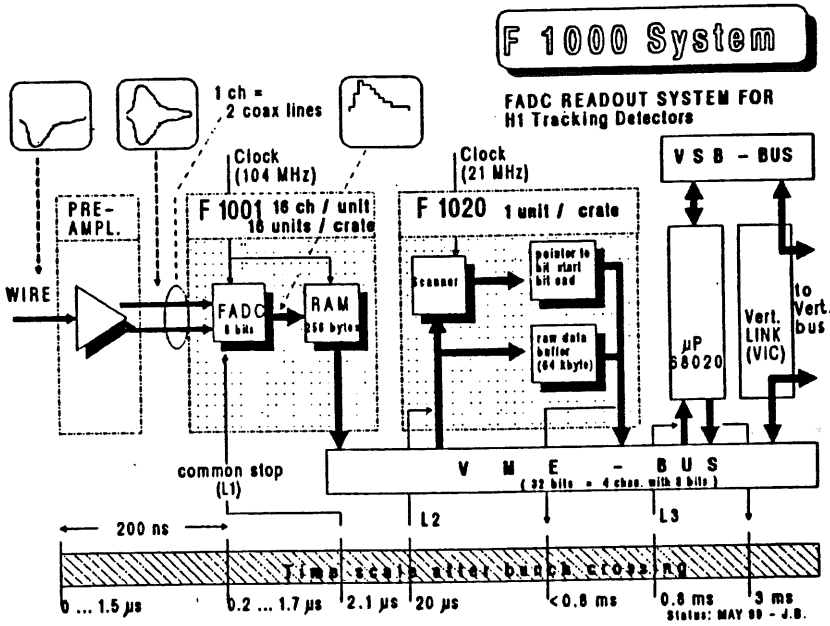


Figure 2.10: Readout system of the H1 drift chambers

L2keep, the scanner starts the serial readout of the FADC memory into a raw data buffer. This transfer takes place in 800 μs at a rate of 80 Mbytes/s and can be interrupted at any time by a L3reject signal which causes the system to start sampling again. Simultaneously, the data are sensed for the occurrence of pulses. Pointers corresponding to time slices where the pulses cross a pre-set threshold are stored in a local memory, the "scanbuffer".

When readout and sampling are completed in a crate, the scanner signals the end of the process to the front-end processor (FEP). Then the FEP will read asynchronously the zero-suppressed data into its memory and analyse them to determine the driftime and the charge of the track space points (Qt analysis). The results are stored in a Qt buffer in the FEP memory. A central processor is then responsible to read this buffer, eventually complemented with the raw data, over a vertical link into the DC master crate. There they are stored in proper order in the DC multi-event buffer.

2.5.3.2 LAr Calorimeter Readout

As was mentioned in section 1.4.1, the calorimetry in H1 uses liquid argon as active medium. Roughly speaking, the calorimeter consists of parallel conducting plates of a dense material interleaved with small gaps filled with liquid argon. Particles traversing the gap ionise the LAr along their tracks (see figure 2.11). The generated free charge carriers are separated and collected on readout pads by

a high voltage field across the gap. The signal is built up by the electrons drifting to the anodes with a constant velocity of around 5 mm/μs. The positive ions of very low mobility do not contribute to the signal charge.

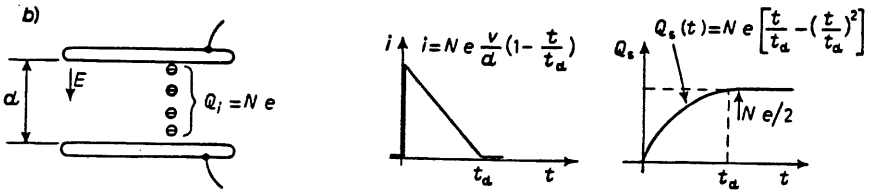


Figure 2.11: Charge collection in the LAr calorimeter due to an uniform ionization in the Ar gap. In the readout configuration of the H1 calorimeter, the charge deposited by a minimum ionizing particle is Q = 18310 e in the hadronic gaps and Q = 9950 e in the e.m. section [29]. The drift time is $\sim$ 500 ns

The 45000 readout pads of the H1 calorimeter are connected through 10 m long transmission lines to an analog signal processing chain mounted on the detector. Each line is first fed into a low noise charge preamplifier followed by a shaping amplifier and a sample and hold (S/H) circuit. This latter acts as an analog memory to store the peak value of the signal during the data acquisition period (see 2.4). Upon a L2keep trigger, the S/H output voltages are collected through multiplexers and digitised in parallel by 14-bit ADCs (see figure 2.12). The ADC counts are read out by over 50 digital signal processors (DSP) which perform zero suppression, pedestal subtraction, gain correction and energy calculations [30], [31]. In each branch, the ADC conversion takes place in 800μs while the DSP encoding is processed in about 1.5 ms. Buffers placed before and after the DSPs limit the first order dead time to the ADC conversion and allow the derandomization of the next readout stages. If the event survives to the L3 trigger, the data are collected from the DSP buffers, combined in an event record and transferred in the calorimeter MEB.

2.5.4 Central Data Acquisition

2.5.4.1 Full Event Building

Full event building is the process of collecting the data from each subdetector MEB and combine the information to form full event records. This process runs under the control of a single VME bus processor, the "Event Coordinator". During data acquisition, its main tasks are to manage the MEB buffers and to initiate DMA block transfers from the different subsystem master crates into the event builder crate.

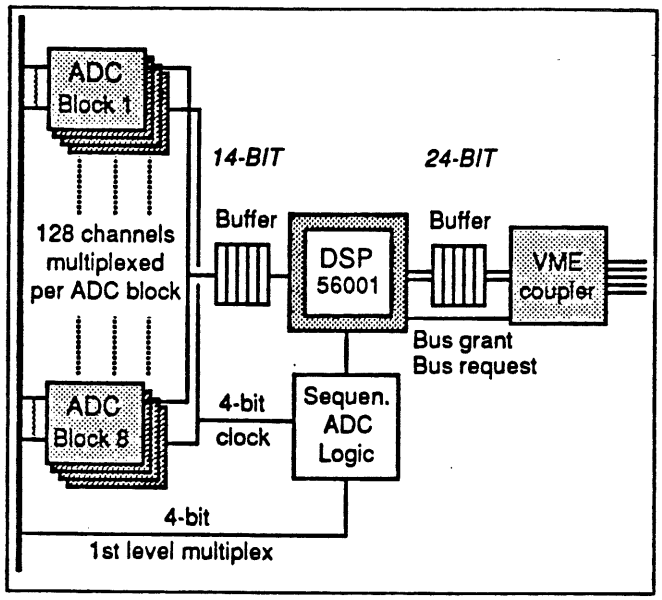


Figure 2.12: Schematic of the H1 calorimeter ADC readout

To sustain a high event building rate, a fast data communication system between the crates is required. Since the subdetector electronics are positionned far from the CDAQ system (± 50 m), an optical fibre link has been chosen to avoid noise and grounding problems. The event builder crate and each subsystem master crate contain a VMEtaxi module from Micro-Research [32] which connects them in a ring type configuration with optical fibres (figure 2.13). The data are transferred over the ring by the AMD7968/7969 Taxichip transmitter/receiver chipset which offers a parallel-channel throughput of 12.5 Mbytes/s over a serial link that operates at 125 Mbits/s [33]. The communication protocol is controlled by an onboard 68020 microprocessor which may also run user applications. For instance, the central event coordinating task runs on the master VMEtaxi of the ring and interacts with each subsystem readout controller via shared memory blocks (see figure 2.14). During acquisition, data are placed by the subsystem controllers into the buffers over the VMEbus and, when all components are ready with the same event number, the banks are broadcast through VSB and via the optical ring into the full-event buffering (FEB) system. The use of the VSB bus in the master crates ensures that the event building task does not interfere with the front-end data acquisition.

Given the different software overheads, this system achieves presently a sustained throughput of 3 Mbytes/s, for 12 subdetector branches and an average event size of 60 kbytes, fixing the maximum event building rate to 50 Hz. An upgrade of the VMEtaxi ring is forseen which should allow to surpass 200 Hz.

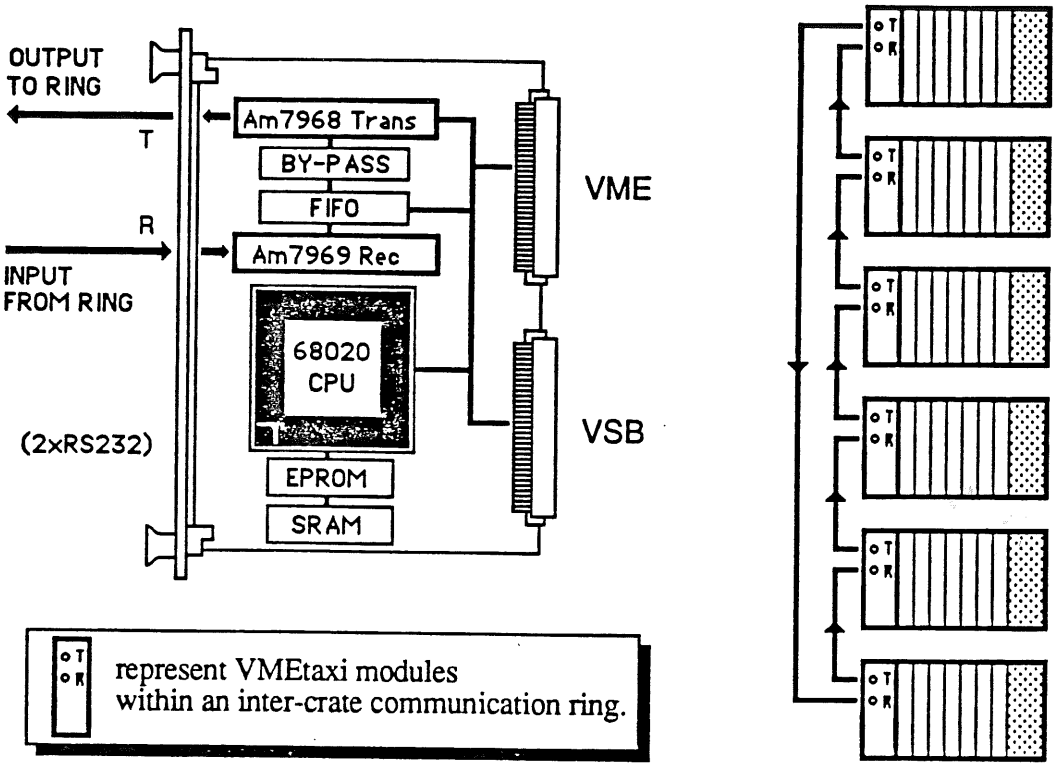


Figure 2.13: VMEtaxi philosophy

2.5.4.2 Full-Event Buffer Units

Each FEB is attached via a VSB connection to a processor and is equiped with extra data links to form a Full-Event Unit associated with an "event task" (figure 2.15). Such tasks include for example data logging, level 4 filtering, event display, data monitoring. The full event data records are put into a FEB memory according to the prevailing CPU request conditions. Each FEB can store two full event records so that reading and filling can be processed simultaneously. A Full-Event Unit can be either a "consumer" of data (e.g. filter input, event display...) or a "producer". They are all under the management of the Event Coordinator. This section describes two of these tasks, the event filtering and the data logging.

The most sophisticated unit is the fourth level event filter which performs the final on-line rejection of background interactions [34]. This unit consists of a set of RAID8235 boards running in parallel an identical copy of the Fortran filter program (figure 2.15). The RAID8235 is a VME/VSB board based on the 25 MHz RISC R3000 processor and the R3010 floating-point unit with up to 32 Mbytes of DRAM. It has an equivalent computing power of about 50% of an IBM 3090 mainframe. Event input and output to the RISC system are controlled independently by two MC68020 based processors boards. When a farm processor node is free, it signals this to the input controller which in turn will request an event from the filter input FEB. When an event is ready for processing, its data

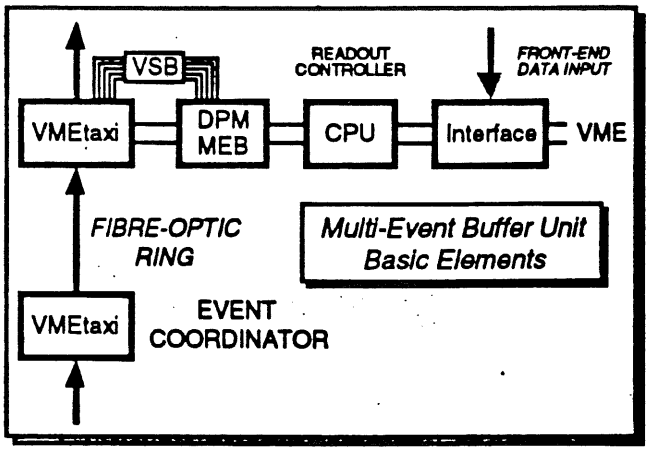


Figure 2.14: Multi-event buffer readout

are extracted by the controller over the VSB and sent to the free RAID. The input controller is then free to service another node. When a node has finished the processing, it adds results banks to the record and signals completion to the output controller. If the event is bad, the controller may tell the node to drop the event and signal that it is free. If the RAID has decided to retain the event for the off-line analysis, then the output controller is responsible for broadcasting the returned event to the feedback FEB memory. Completion of this transfer is signalled to the farm input controller which may then request a new event for the node. This configuration allows an average processing rate of $\sim$ 6 Mbytes/s.

An other typical full-event task is the data logging. Final event records are sent to the DESY Central IBM facility, some 3 km distant from the H1 experimental hall, over an optic fibre link. Disc writing limits presently the system to 1.2 Mbytes/s but rates up to 7 Mbytes/s are possible over the link. In case of a link failure, a backup task that drives a storage device directly from VME can be enabled.

2.5.5 Overall Experiment Control

The readout chain described above runs as a stand-alone system during data acquisition. However external computing stations are needed to supplement the tasks performed by the VME processors for system initialisation and supervision, data monitoring and also for software development and testing. Within H1, over 30 personal computers and workstations are integrated in the VMEbus environment for this purpose. Emphasis has been placed on the use of the Apple Macintosh II computer family (MAC II ci, cx, fx) based on the 68020/68030 microprocessors. This computer features an open NuBus slot expansion cage which permits the

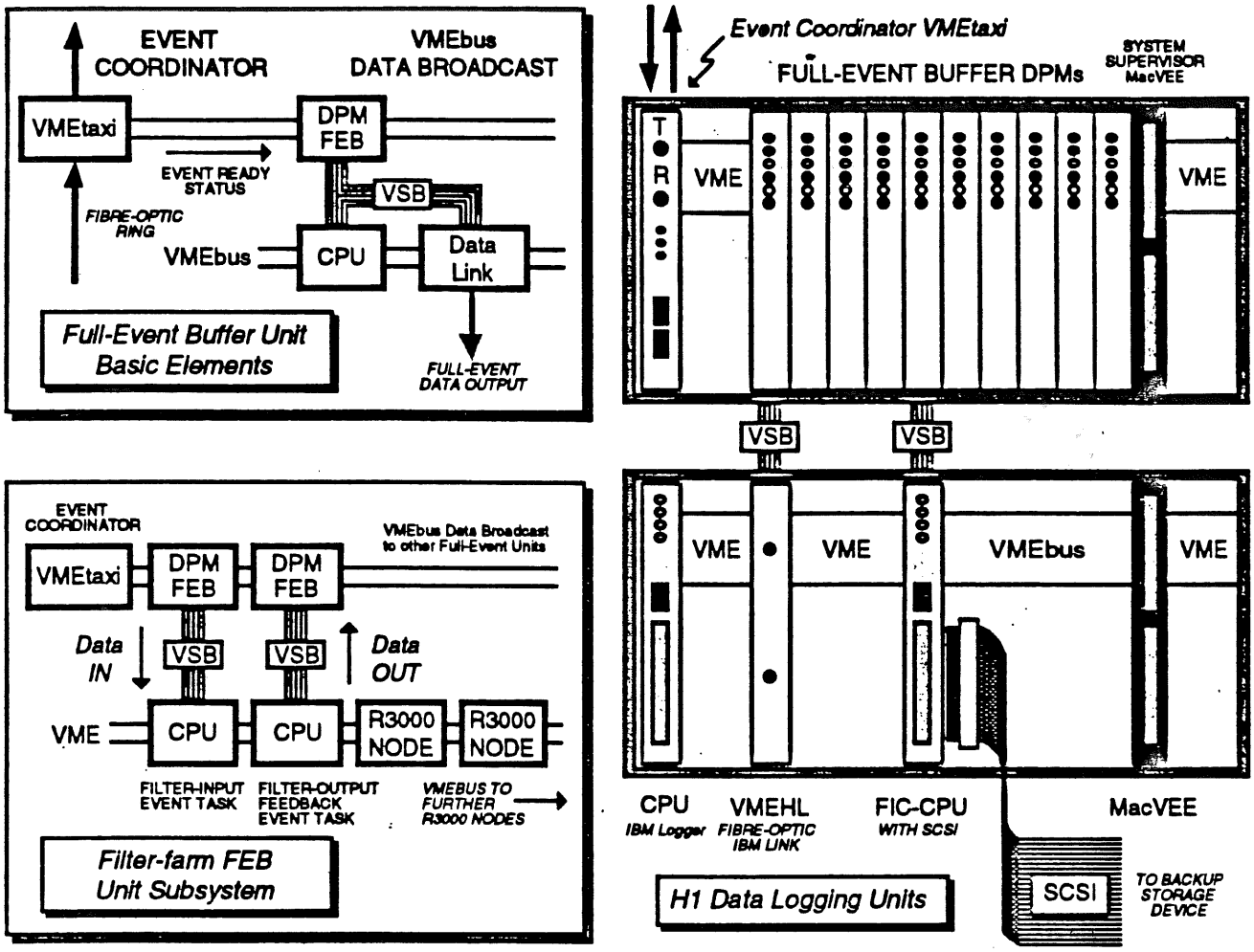


Figure 2.15: Full-event buffer units

central processor to access external systems through plug-in boards. Particularly, the VMEbus may be mapped into the address space of the computer processor such that the Macintosh acts as a VME master.

Different Macintosh II - VMEbus interfacing systems have been developed. The most commonly used in the high energy physics environment, and therefore in H1, is the MICRON/MacVee system [35] which allows to connect up to 8 VME crates. These interfaces support all standard VME data transfer operation types and automatically perform the required VME operations, so that no special software drivers are necessary. As a result, the object code of programs running on VME CPU boards can be developed on the Macintosh and no operating system is required on the VME boards. A simple debugger/monitor facility [36] is sufficient to enable the basic CPU functions, such as CPU start, stop, abort..., via external directives through a terminal port or mailbox memories mapped on the

VMEbus. This solution allows to run data acquisition tasks without inhibiting kernels limiting the potentialities of the hardware structure. On the Macintosh, software are written into the Macintosh Programmers Workshop (MPW) environment [37] which provides Assembler, Pascal, C and Fortran compilers. Special tools have been developed to easily execute VME accesses [38]. For the development of run-time applications, such as system supervising and data monitoring, the Super Card and MacApp packages are extensively used.

Other types of workstations are employed when program development and large data storage require more powerful computers. For instance, VAX workstations are used in the calorimeter area whereas the code for the filter farm is prepared on a MIPS M/120-5 computer under the UNIX operating system. All these stations are connected to an Ethernet network to allow exchange of information and data files between the different systems.

Chapter 3

Detection and Signal Processing in the MWPC System

3.1 Introduction

The signals from all MWPCs installed in the H1 tracking detector are processed in a distinct branch of the H1 data acquisition system. A dedicated linear chain and readout system have been developed to transmit the information from the 4000 MWPC sensing channels to the central event builder. Table 3.1 summarizes the principal characteristics of the chambers relevant for the data acquisition. Three detectors, FPC, CIP and COP, have a capacitive cathode pad readout whereas the backward detector has anode wire readout.

Detector	*Layers*	*Readout type*	*Channels*
Forward prop. ch. (FPC)	6	Cathode pad	1152
Central chambers (CPC):			
inner (CIP)	2	Cathode pad	960
outer (COP)	2	Cathode pad	576
Backward prop. ch. (BPC)	4	Anode wire	1248
Total			3936

Table 3.1: MWPC system

The function of the MWPCs in the H1 detector does not require a precise

charge measurement. An 1-bit discrimination based on the pulse amplitude is sufficient to extract the track space point information used to locate the primary interaction vertex and to support the track reconstruction. To identify properly the event occurrence time t_0, an accurate synchronization with the bunch crossings in the collider is essential before the trigger processing and the pipelining of the data.

This chapter gives a description of the MWPC analog chain and the associated front-end receiving electronics. In sections 3.2 and 3.3, the principles of particle detection in a multiwire proportional chamber and the capacitive readout technique are described. Section 3.4 gives an overview of the front-end signal processing. The pulse amplification and shaping are detailed in 3.5 while the components used for the digitisation, the synchronization and the pipelining are described in 3.6.

3.2 Fundamentals of Particle Detection in Multiwire Proportional Chambers

A multiwire proportional chamber usually consists of a set of equally spaced anode wires, sandwiched between two cathode planes and filled with a suitable gas. When a positive high voltage is applied on the anode wires, the cathodes being grounded, an electric field develops as illustrated in figure 3.1. In the major part of the

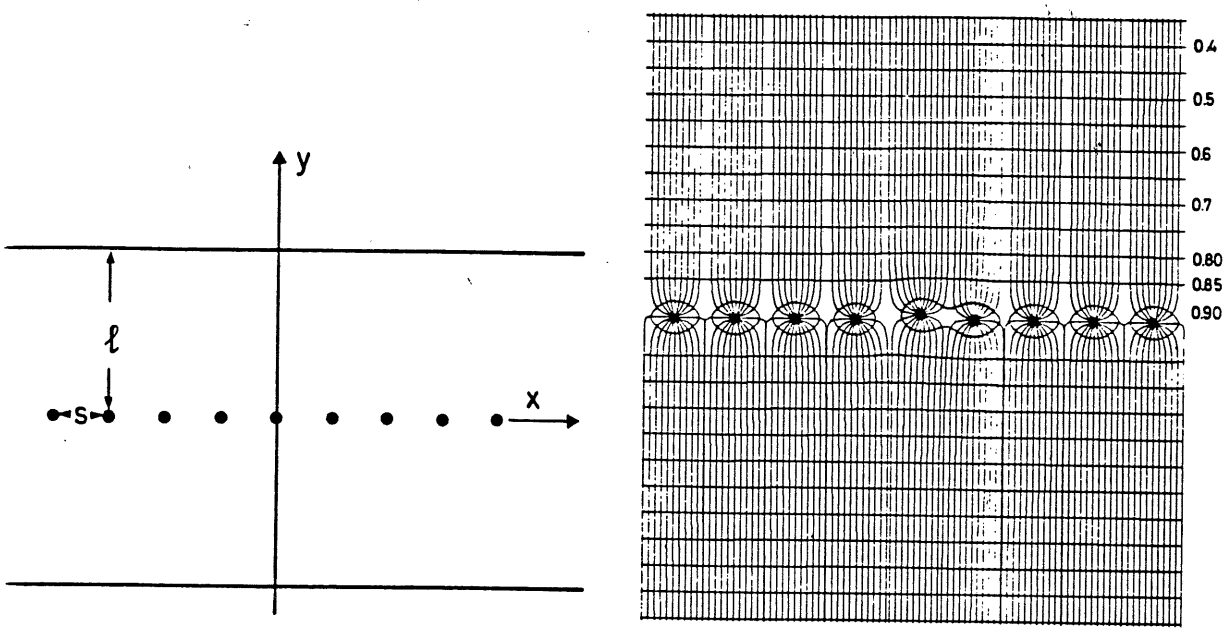


Figure 3.1: Electric field equipotentials and field lines in a MWPC

chamber the field is uniform, but close to the wire it is almost identical to the field

of an independent cylindrical counter (E $\propto 1/r$). The electrons liberated in the gas by an ionizing particle drift along the field lines toward the high field region. Very close to the anode, at a distance of a few wire radii, the field gets strong enough so that the electrons experience inelastic ionizing collisions, forming a multiplication avalanche surrounding the wire. The electrons are collected on the anode and the positive ions drift to the cathodes. The whole process of multiplication and electron collection takes place in about 1 ns.

The detected signal is the consequence of the motion of the charges liberated in the gas in the electrostatic field. A negative pulse is obtained on the anode wire and complementary to this, there is a positive signal on the cathodes. Since almost all the ion pairs are formed very close to the anode wire, the electrons travel only through a small fraction of the total potential and their contribution to the signal is very small. It is the motion of the positive ions that generates most of the signal.

The time development of the induced charge signal on the electrodes can be obtained by computing the electric field in the chamber in the presence of point charges moving to the cathodes. Around the anode wire ($y << s$) the field is radial and the expression obtained for a cylindrical counter may be used, provided that the correct value for the capacity is used [39]:

$$Q(t) = \frac{Ne}{2}\frac{C}{4\pi\varepsilon_0} ln(1+\frac{t}{t_0}) \tag{3.1}$$

$$i(t) = \frac{dQ(t)}{dt} = \frac{Ne}{2}\frac{C}{4\pi\varepsilon_0}\frac{1}{(t+t_0)} = \frac{i_m}{1+t/t_0} \tag{3.2}$$

where

$$t_0 = \frac{\pi\varepsilon_0 a^2}{\mu^+ C V_0} \tag{3.3}$$

with N number of positive ions leaving the avalanche site (gas amplification).
C capacitance per unit length of the chamber:

$$C = \frac{2\pi\varepsilon_0}{(\pi l/s) - ln(2\pi a/s)} \tag{3.4}$$

l semi gas gap
s wire spacing
a anode radius
ε_0 permittivity of free space
μ^+ positive ion mobility
V_0 static anode voltage

Different assumptions have been made to derive these expressions that limit their application. Particularly, at very short times ($t/t_0 < 1$), discrepancies arise due to the electron component and from the dependence of the ions mobility on the field near the anode. Furthermore, the actual waveform results from the superposition of the responses of the multiple ($\sim$ 25) ionizing collisions along the track.

As an example, let us consider the signal development in the COP detector. The basic set of conditions are:

i) chamber geometry. a = 10 μm, s = 2 mm, l = 4 mm.

ii) operation conditions. gas: 50% Ar + 50% C_2H_6, positive ion mobility μ^+ taken as $10^4\ m^2v^{-1}s^{-1}$, V_0 = 3 kV.

It follows that C = 5.7 pF/m and t_0 = 1.6 ns. The current and charge waveforms as functions of time are illustrated in figure 3.2.a. An abrupt rise of the

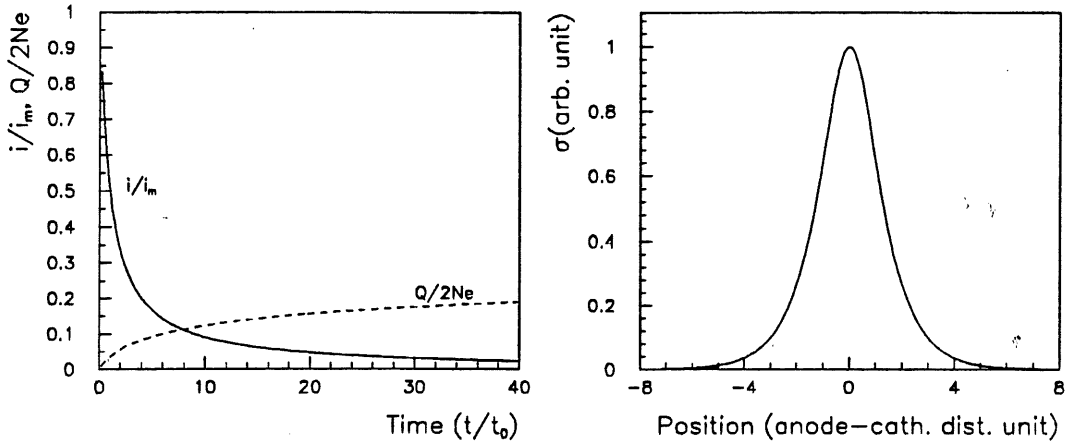


Figure 3.2: a) Approximated induced current and charge waveforms on the cathodes of the COP detector. b) Charge density distribution on the cathode.

current is physically not possible and is constrained by the maximum velocity of the positive ions and other broadening terms, such as the time extent of the avalanche. The important feature is that a substantial fraction of the charge is collected in a short time, a few t_0. This provides the ability to operate the counter at high counting rate by observing only the early part of the signal ($t/t_0 \leq 5$) and by cancelling the long tail by pulse shaping in the readout electronics.

The charge density $\sigma(x, z)$ on the cathodes in the first nanoseconds is obtained by calculating the electric field on two parallel conducting planes due to a static

charge $Q = Ne$ sitting on an anode wire at $x, y, z = 0$ [40] :

$$\sigma(x,z) = \varepsilon_0 \, E(x,z) = -\frac{Q}{2\pi} \sum_{n=0}^{\infty} (-1)^n \frac{(2n+1)\, l}{\{l^2(2n+1)^2 + x^2 + z^2\}^{3/2}} \tag{3.5}$$

The projection on the x axis is obtained by integrating over z:

$$\sigma(x) = \int_{-\infty}^{\infty} \sigma(x,z)dz = -\frac{Q}{4l} \, (\cosh \frac{\pi x}{2l})^{-1} \tag{3.6}$$

This distribution is plotted in figure 3.2.b with the x position measured in units of the anode-cathode distance (i.e. $l_{CIP} = 3\ mm$, $l_{COP} = 4\ mm$). Equation (3.6) can be used to estimate the hit multiplicity for particles traversing the chamber near a pad boundary or under an angle $\neq 90^o$ with respect to the chamber axis. A discussion of this topic for the CIP detector can be found in [13]

3.3 Signal Detection in the Central and Forward Chambers

In the central and forward MWPCs, the localisation of the avalanche along the anode wires is based on the detection of pulses induced on pick-up electrodes outside the gas volume. This electrode arrangement has attractive advantages over standard cathode readout where the same electrode performs the double function of cathode and detection element. For instance, the segmentation possibilities are widely extended and the readout connections are simplified. In this section, we discuss the principle of operation of this readout method, with the readout arrangement of the COP detector taken as example.

3.3.1 Readout Cell

The basic geometry of the COP readout structure is shown in figure 3.3. As already mentioned in chapter 1, the cathode is made of a 25 μm thick kapton foil coated with a resistive graphite paint on the side facing the anode wire plane. The outer surface of the cathode is glued to a second kapton foil carrying a set of $12 \times 20\ cm^2$ copper strips. The latter are connected to preamplifiers by 50 μm diameter copper wires through a 3 mm thick Rohacell layer. The signals propagate over transmission lines formed by the copper wires and the external kapton-copper foil glued on the Rohacell. The electrical connections are also shown in figure 3.3. The strips are grounded via the input resistance R_{in} of the preamplifier. The cathode as well as the external copper layer are also grounded. The anode wires are connected to a positive high voltage.

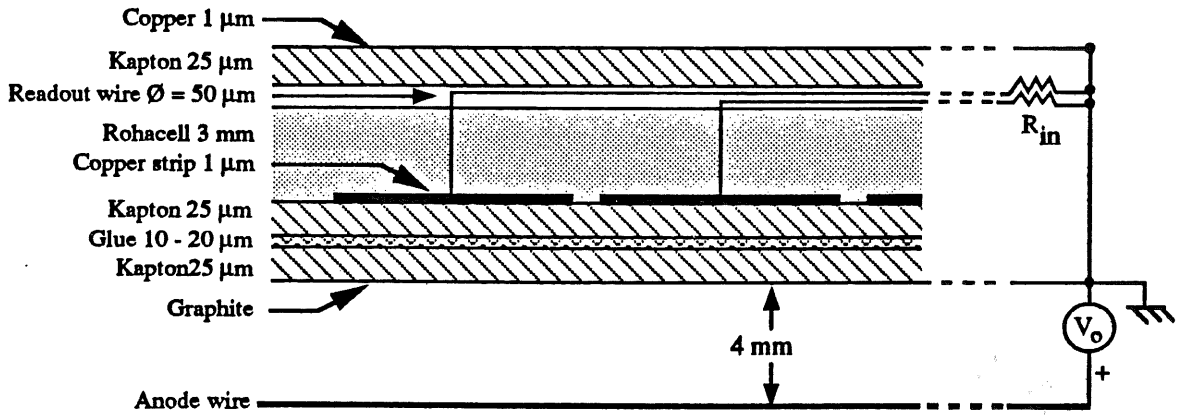


Figure 3.3: Transversal view of the COP readout structure

If the resistivity of the graphite coating is high enough, the cathode is transparent to transient fields and a signal induced by the motion of the ions in the gas volume may be detected outside the cathode. The order of magnitude of the minimum cathode surface resistivity required for full transparency is around 10^5 Ω/square[1] [41]. A value in the range $10^5 - 10^6$ Ω/square is usually chosen (e.g. forward MWPCs : 100 k$\Omega/\square$, COP : 200 k$\Omega/\square$, CIP : 400 k$\Omega/\square$). A higher resistivity can produce a reduction of the average pulse height at high counting rate. Indeed, in that case the charges collected on the cathode are no longer eliminated to ground giving rise to a distortion of the electrostatic field. It must be also noted that only a fraction of the signal transmitted through the cathode is absorbed in the copper strips. Indeed, the thickness of the Cu (1 μm) is smaller than the skin depth for frequency up to 4 GHz out of the range in which we are working.

3.3.2 Transmission Lines

The signal absorbed in a strip propagates over a transmission line approximately matched to the input resistance of the preamplifier to avoid pulse distortion. If the line resistance and the dielectric loss are neglected, the characteristic impedance of the transmission line is given by:

$$Z_l = \frac{1}{2\pi}\sqrt{\frac{\mu_0}{\varepsilon_0\varepsilon_r}}\cosh^{-1}(ca^{-1}) = 48\ \Omega \qquad (3.7)$$

[1]The cathode resistivity is measured with two rectangular electrodes of height h (e.g. 10 cm) which are spaced at a distance h. In the following, the surface resisitivity is noted $\Omega/\square$.

where

a is the readout wire radius (25 μm)
c is the distance of the wire to the copper surface (50 μm)
ε_0 is the permittivity of free space
ε_r is the relative permitivity of kapton (3.5)
μ_0 is the permeability of free space.

The intrinsic line capacitance and inductance per unit length are:

$$C_l = 2\pi\varepsilon[\cosh^{-1}(ca^{-1})]^{-1} = 148\ pF/m \tag{3.8}$$

$$L_l = Z_l^2 C_l = 260\ nH/m \tag{3.9}$$

The propagation delay is:

$$T_{pd} = \sqrt{L_l C_l} = 6.2\ ns/m \tag{3.10}$$

It should be noted that these formulae give only approximate values in the case of a very thin dielectric (a $\approx$ c). However more accurate predictions have no sense because of the uncertainty on the glue thickness.

3.4 Front-end Signal Processing

The transmission lines and the anode wires of the BPC are connected to preamplifiers which are soldered on printed circuit boards mounted on the chamber end flanges (see figure 3.4). The differential outputs of the preamplifiers are connected through 35 m long cables to the Receiver Cards located in the electronic trailor. There, each differential line pair is connected to a shaping amplifier which contains a cable terminator, a differential amplifier and a pulse forming network. The shaped pulse is digitised by a voltage comparator, with an adjustable threshold in an 1-bit value. If the pulse amplitude exceeds the threshold voltage, a TTL pulse with a width equal to the time-over-threshold is generated.

At the output of the discriminators, the leading edge of the TTL pulses related to a given bunch crossing are distributed in time as illustrated in figure 3.5. These distributions are essentially the superposition of the intrinsic chamber time jitter (see figure 1.14) and of the different propagation delays over the transmission lines. A fixed delay of about 190 ns must be added to take account of the propagation time over the cable (5.1 ns/m) and through the various analog components. To restore the time correlation between event signals and the bunch structure of the HERA machine, the discriminator output is fed into a dedicated synchronizer

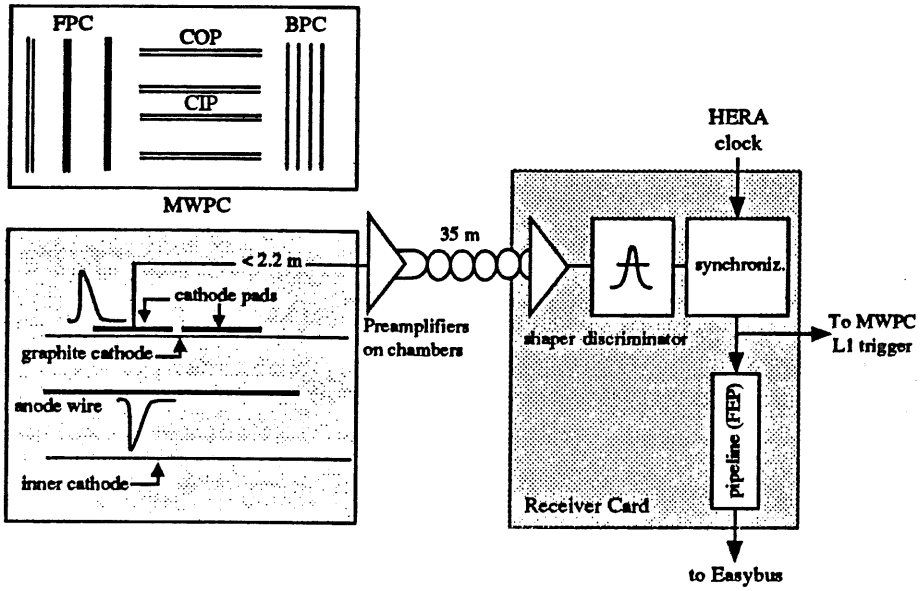


Figure 3.4: Overview of the MWPC front-end electronic chain

circuit driven by a 10.4 MHz clock with a fixed phase relative to the collider clock signal. If a pad or a wire fires at a given bunch crossing time t_0, this circuit will generate at time t_0 + 340 ns a synchronized 96 ns long digital pulse (see 3.6.3). This pulse is distributed to the Z-vertex and forward ray finder trigger logics and fed into a 30-stage shift register (pipeline) clocked with the 10.4 MHz frequency.

During the preparation of the L1 decision, the data propagate to the output of the pipeline, leaving entries for new data at the input. If the event is rejected by the L1 trigger, the data are just dropped out of the pipeline after 30 HCk cycles. If on the other hand, a L1keep is received the propagation in the pipeline is stopped about 2.3 μs after the event occurrence. At that time, the data which caused the L1keep are latched in the 22nd stage of the pipeline register. They are then shifted automatically over a certain number of stages. The number of stages over which the data are shifted is determined by the "event history" that is requested for the analysis, i.e. the number of BC's before and after the time slice that contains the "triggered" data. The system then waits for the L2 decision. In the case of a L2reject, the pipeline is simply cleared and reopened to accept new events. On the other hand, if the event is kept for further filtering, the readout of the pipelined data into a FIFO buffer is initiated.

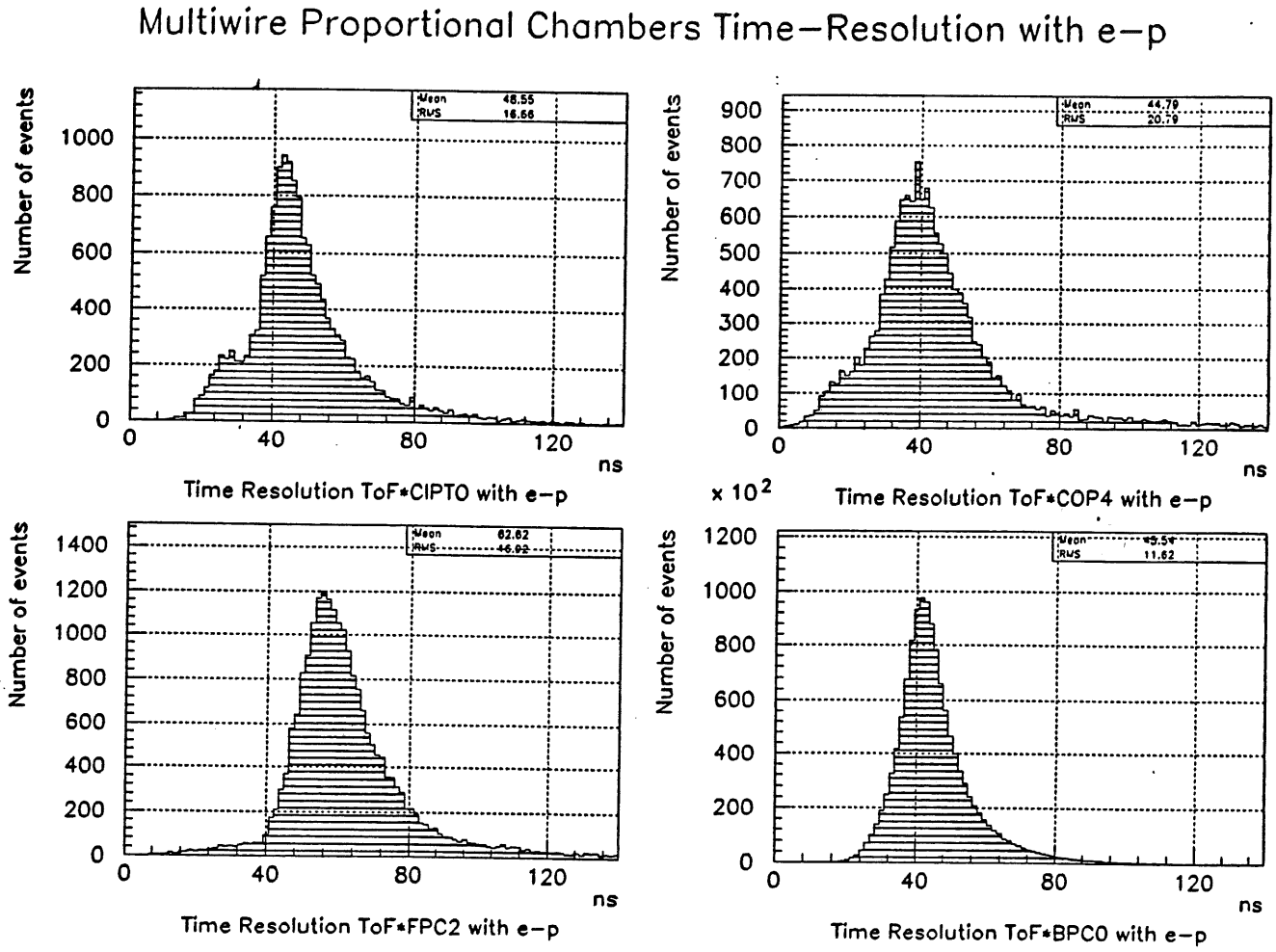


Figure 3.5: Time distribution of the MWPC signals as measured on the Receiver Card before synchronization with the collider clock signal HCk.

3.5 Amplification and Pulse Shaping

3.5.1 Principles of the Analog Signal Processing

The detected signal in a proportional counter is the consequence of the motion in the electrostatic field of the positive ions liberated in the avalanche around the anode wire. The electrode on which the signal is sensed represents a capacitance C_D to ground, so that from the signal processing point of view the detector can be considered as a capacitive current source $i_d(t) = i_m/(1 + t/t_0)$ (see figure 3.6). The value of C_D is obtained by considering all the shunt capacitors of the readout electrode to ground and is typically 20 pF/m [42].

The charge induced on the electrodes is measured by discharging the detector into a charge sensitive amplifier. For this purpose, a common-base amplifier has been chosen. This configuration has the advantages of well defined low input

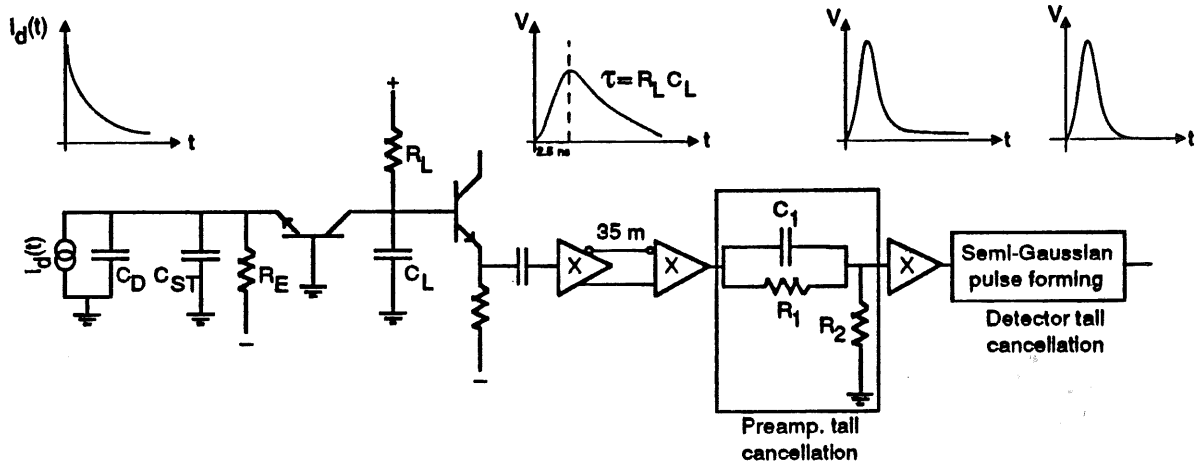


Figure 3.6: MWPC analog signal processing chain

impedance (25 - 100 Ω) and very fast impulse response (~ 1 ns rise time). It is used when the pulse shape of the input signal has to be correctly reproduced. The input impedance is given by $R_{in} = 26/I_E$ (mA) where I_E is the emitter current in the common-base transistor. It may be adjusted so that the transmission line between the readout pad and the preamplifier is correctly matched. The detector current is integrated on the capacitance C_L of the collector node to ground and converted in this way in a voltage signal with an amplitude proportional to $1/C_L$. The signal rise time is determined by the charge transfer speed into the common base stage, i.e. by the input time constant τ_{in}:

$$\tau_{in} = R_{in}(C_D + C_{ST}) \simeq 50\ \Omega \times 50\ pF = 2.5\ ns \qquad (3.11)$$

where $C_{ST} \simeq 2 - 10$ pF includes all the stray capacitances at the input of the first transistor. The decay in the voltage response is due to the collector load resistance R_L. In hybrid technology, C_L can be as low as $1 - 2$ pF, resulting in a $R_L C_L$ time constant of ~ 10 ns for typical values of R_L (~ 5 $k\Omega$).

The output of the common base stage is connected via an emitter follower circuit to a differential cable driver that transmits the signal through a 35 m long cable from the detector to the readout electronics. There, the signal is received in a shaping amplifier ("shaper") which provides additional voltage gain and shorts the trailing tail of the detector and preamplifier responses.

The pulse shaping consists functionally of two parts. First, the signal passes through a pole-zero cancellation circuit that replaces the exponential decay shape by a shorter one. This filtering is implemented with a high-pass RC network that differentiates the preamplifier response with a short time constant R_2 C_1. The undershot produced by the differentiation of the trailing edge is cancelled by adding a fraction of the original signal through R_1. The second stage of the

shaper amplifier consists of a semi-Gaussian pulse forming network. Its function is to reduce the effects of pulse overlap at high counting rates and to minimize the measurement error with respect to noise. It can be shown [43] that a filter with a Gaussian impulse response provides the optimum filtering of the noise of charge preamplifiers. This type of filtering may be approached for instance by a cascade connection of a RC differentiator and (n − 1) integrators with the same time constant τ. The impulse response of such a filter is a Poisson (or semi-Gaussian) function of the nth order h (t) = $(t/\tau)^n \exp(-t/\tau)$.

3.5.2 The Preamplifier

The preamplifiers are thick film hybrid circuits containing 1 channel per board. They are soldered by group of 12 (COP), 15 (CIP) or 16 (FPC,BPC), on printed circuit motherboards mounted on the end flanges of the chambers. Two types of preamplifiers [44] have been developed, one is used for cathode pad readout (CIP, COP, FPC), the other for anode wire readout (BPC). The circuit diagrams are given in figure 3.7 and the main characteristics are listed in table 3.2. The two

Differential gain	65 nV/e^-
Rise time (10 - 90%)	2 ns
Fall time (10 - 90%)	20 ns
Input impedance	64 Ω
Output load	2×50 Ω
Dynamic range	± 300 mV (∼ 10^7 e^-)
Power supply	± 3.5 V (22 mW)
Size	25.4 × 10 × 2 mm^3

Table 3.2: Characteristics of the MWPC preamplifier

designs are similar except that the cable drivers have opposite polarities. This configuration allows to connect both types of preamplifiers to the same readout chain.

The preamplifier features a test input with a ∼ 1pF capacitor by which a charge may be injected into the input stage of the circuit. In the final assembly of the readout electronics, the test input is connected to a pulse generator on the Receiver Card. Two test pulses are transmitted to the chamber. One is synchronized on the rising edge of the generator trigger signal (slow 3 signal, see 4.6.4), the other on the falling edge. On the detector, they are connected alternately to the preamplifiers

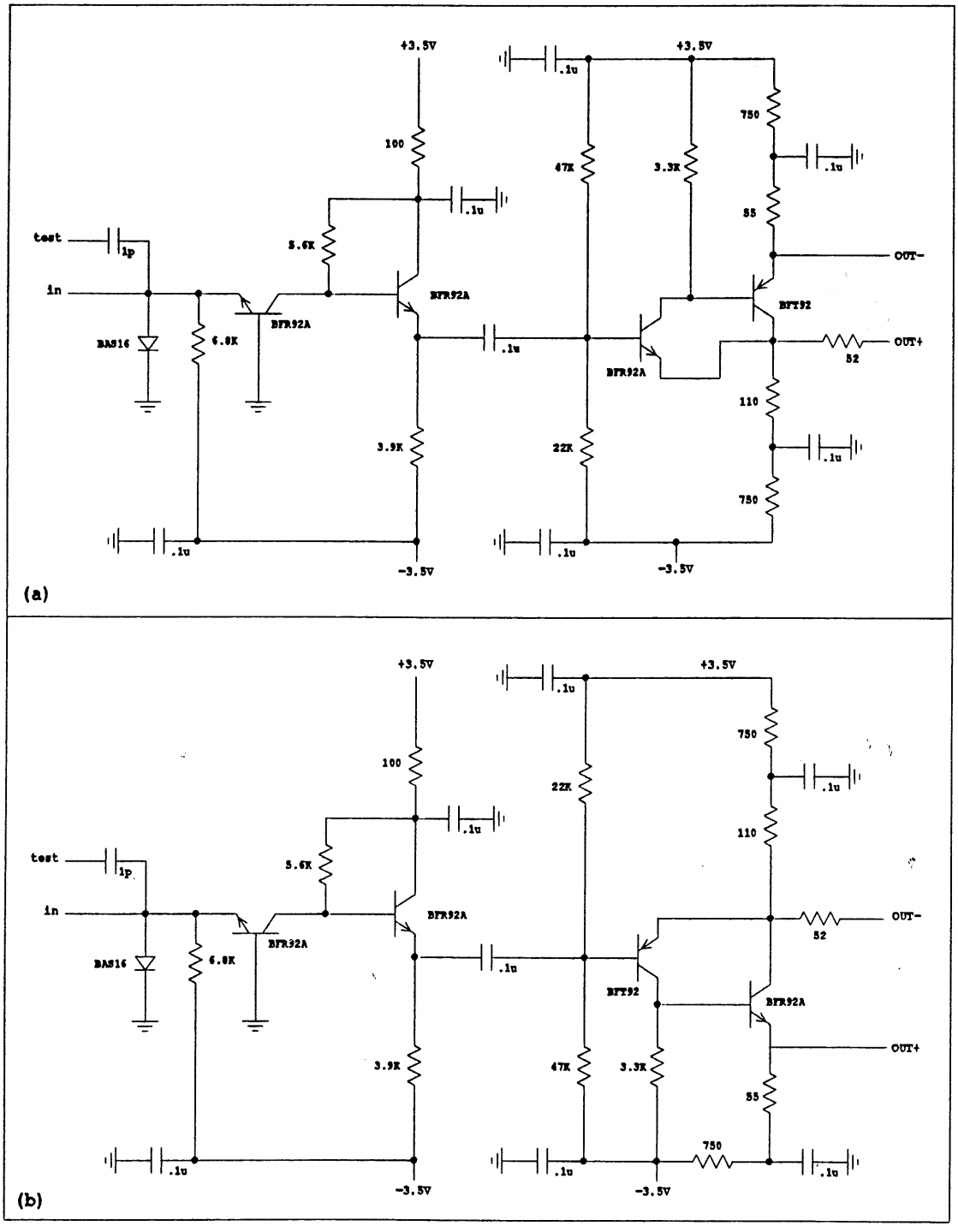


Figure 3.7: Circuit diagrams of the MWPC preamplifiers. a) pad readout, b) anode wire readout

so that even and odd numbered channels are pulsed separately. In this way, the cross-talk between adjacent channels may be measured. The amplitude of the signal at the test input is adjustable by software on the Receiver Card. Figure 3.8 shows the response of the preamplifier to the a voltage step on the test input.

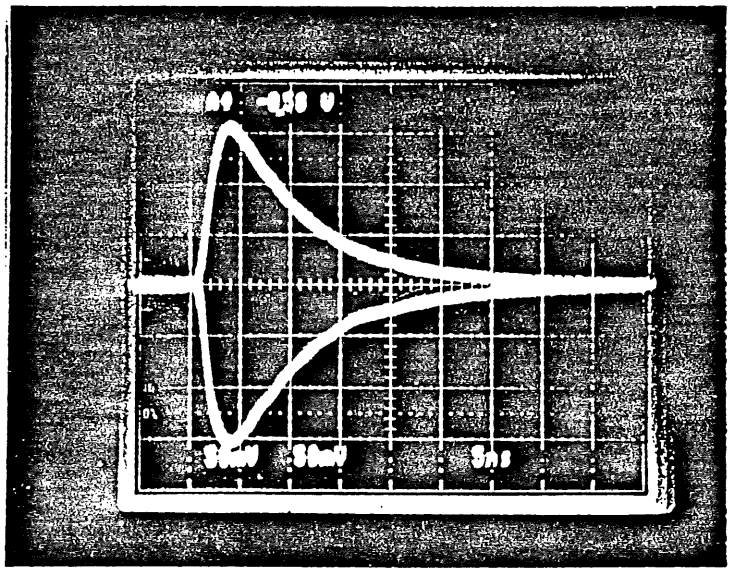


Figure 3.8: Preamplifier response to a voltage step on the test input equivalent to a charge of 5 $10^6 e^-$.

The supply voltages of the preamplifiers (± 3.5 V) are derived from a ± 8 V linear power supply driving a power regulator. Two line pairs in the signal cable are used to carry these voltages to the preamplifiers. A remote-sensing regulation allows to compensate the voltage drops in the cable and on the motherboard.

3.5.3 The Shaping Amplifier

The circuit diagram of the shaper is given in figure 3.9 and its main characteristics are listed in table 3.3. The differential signals are received through a high-pass RC filter which matches the cable impedance. The common-mode rejection is performed by a differential video amplifier (NE592) with a voltage gain adjustable by the use of an external resistor R_G connected between the IRG and ORG pins. The amplification has been measured to vary as $6485 R_G^{-0.84}$ (see figure 3.10). The value of R_G is selected so that the distribution of the pulse height matches the discriminator threshold range without saturation of the shaper. Table 3.4 gives the value of R_G and the corresponding total amplification (preamplifier + shaper) for each subdetector.

The shaper provides two outputs with positive polarity. The OUTAC output is connected to the discriminator. It has a blocking capacitor which allows the adjustment of the DC level at the threshold voltage applied on the INBIAS pin. The OUTDC output is connected through a 100 Ω-termination resistance to a test-multiplexer (see 3.6.5). The signal at the shaper OUTAC output is shown in figure 3.11.

Maximum differential gain	400
Rise time	9 ns
Full width at half maximum (FWHM)	16 ns
Max. output voltage $V_{max} = gV_{in\ sat}$	3.2 V
Overload recovery:	
$V_{in} < 5 \times V_{in\ sat}$	70 ns
$V_{in} = 10 \times V_{in\ sat}$	100 ns
$V_{in} = 20 \times V_{in\ sat}$	120 ns
$V_{in} = 30 \times V_{in\ sat}$	170 ns
Power supply	+ 5 V/−5.2 V, 320 mW
Size	$36 \times 14 \times 3.6$ mm^3

Table 3.3: Characteristics of the MWPC shaper

Detector	R_G (Ω)	Total gain (μV/e$^-$)
FPC	1000	1.30
CIP	470	2.45
COP	330	3.29
BPC	1000	1.30

Table 3.4: Amplification in the different readout partitions.

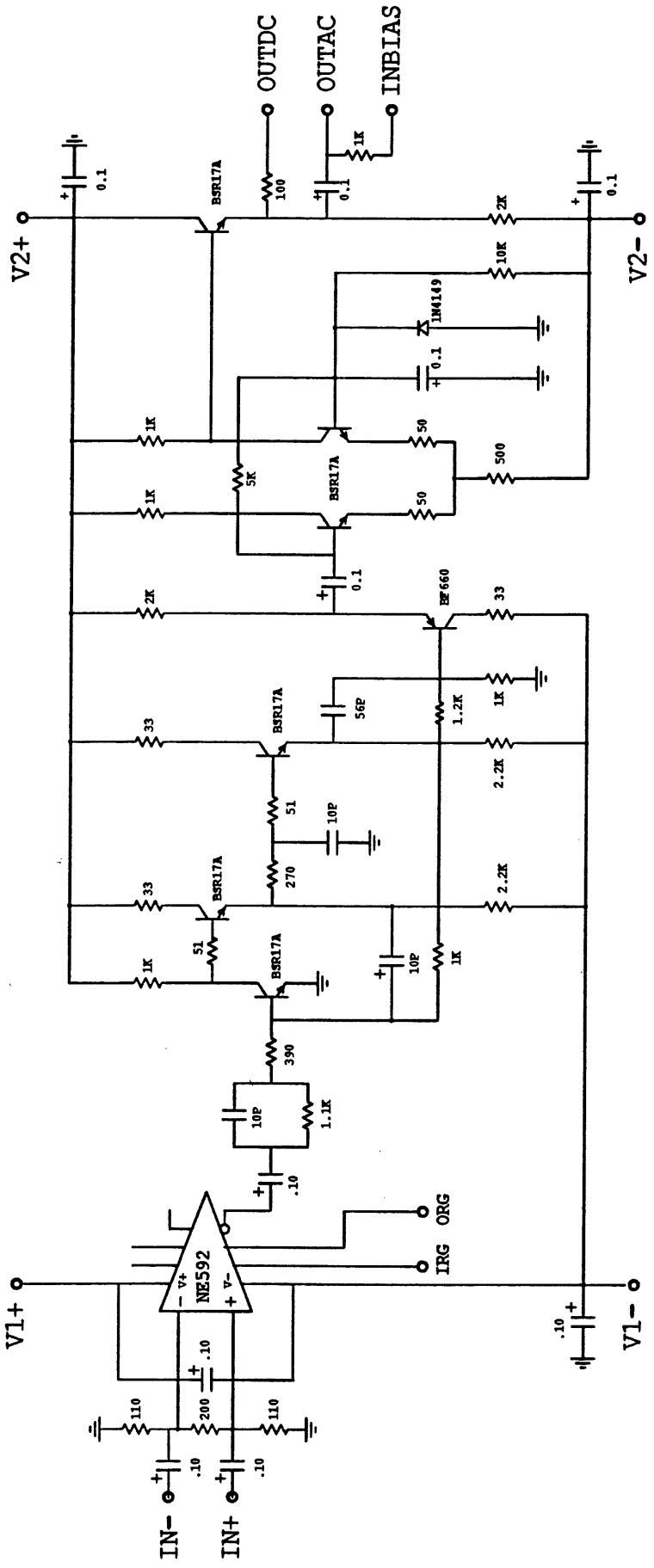


Figure 3.9: Circuit diagram of the MWPC shaper

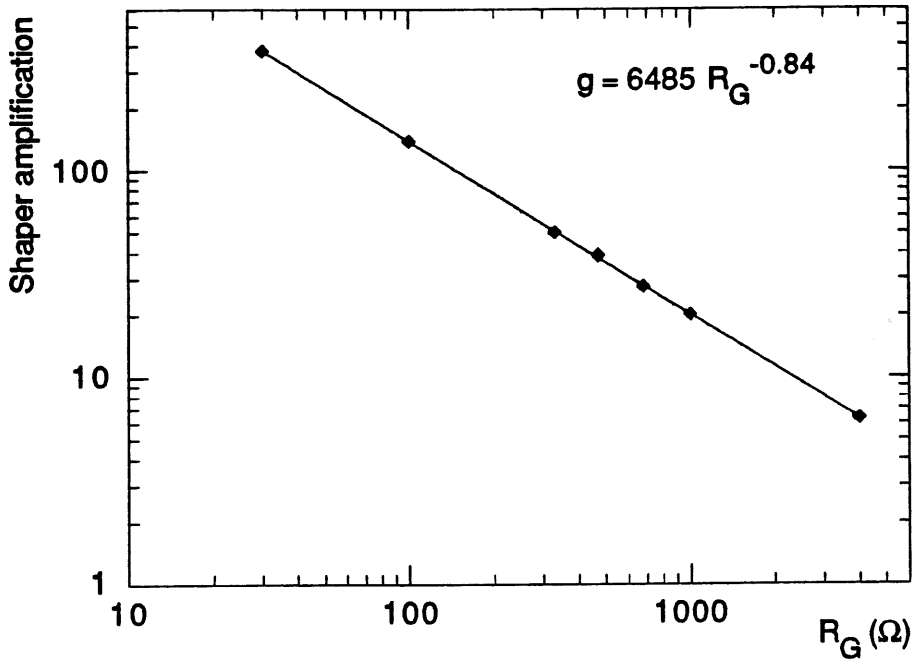


Figure 3.10: Shaper gain as a function of R_G

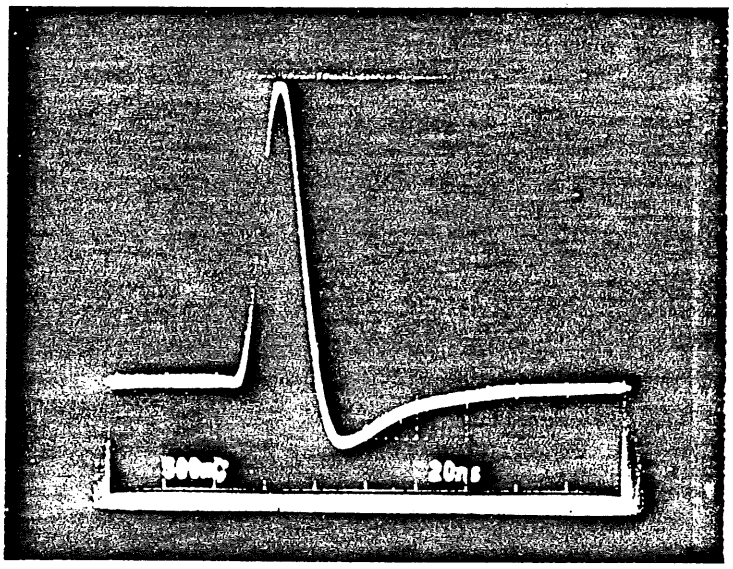


Figure 3.11: Shaper response to a voltage step on the preamplifier test input ($Q = 10^6 e^-, g = 37$).

3.5.4 Noise Considerations

The limit of the detectability of weak signals is set by the amplitude of the noise at the output of the analog chain. One source of noise is the electronic noise that affects the various circuit components in the amplifier. A detailed analysis of the behaviour of the common-base current amplifier is given in [45]. It is shown that the main noise contribution at the time scale of the measurement (10 ns) is due to random potential fluctuations in the conducting channel of the first stage (series noise). This intrinsic noise is conventially expressed by the "equivalent noise charge (ENC_s)" which is equal to the genuine charge that would produce the same signal that the rms of the output noise amplitude distribution. It is given by:

$$ENC_s^2 = 2kTR_sC_{in}^2 \int_{-\infty}^{\infty} [h'(t)]^2 dt \qquad (3.12)$$

where $h(t)$ is the impulse response of the shaper, C_{in} the detector-amplifier capacitance and R_s the equivalent series noise resistance for a bipolar transistor:

$$R_s = \frac{1}{2g_m} + r_{bb'} \qquad (3.13)$$

The transconductance g_m is the voltage-to-current gain $dI_c/dV_{BE} = I_c^2/kT \simeq 1.5\ 10^{-2}\Omega^{-1}$ and the base ohmic resistance $r_{bb'}$ is $\sim$ 30 Ω. If $h(t)$ is approximated by a triangular function,

$$h(t) = \begin{cases} 1 - |\,t\,| / t_m & \text{for } |\,t\,| \leq t_m \\ 0 & |\,t\,| \geq t_m \end{cases} \qquad (3.14)$$

where t_m=10 ns is the zero-to-peak time, then the integral in 3.12 is equal to $2/t_m$ and the ENC for the series noise is

$$ENC_s^2 = 4kTR_s \frac{C_{in}^2}{t_m} \simeq (3800\ \epsilon^-)^2 \qquad (3.15)$$

Another source of spurious output signals is the radio frequency interferences and the "ground loops" in the electrical circuits. They can be reduced or eliminated by an appropriate grounding of the components and a proper shielding of the signal lines, particularly on the detector where low-level signals are processed. A careful attention to the wiring configuration is also required to avoid currents flowing through a ground line. Indeed, a variation in the ground potential may generate a signal in the amplification stages of the circuits and therefore may produce unwanted voltage fluctuations that obscure the desired signal. As an example, the simultaneous switching of the numerous cable drivers distributing the HERA clock to the electronics mounted on the detector induces a clearly observable 10.4 MHz noise component. Consequently, higher discrimination thresholds must be set to separate the noise signals from the genuine chamber pulses leading to a degraded detection efficiency.

3.6 The Receiver Card

This section provides a description of the architecture of the Receiver Card (RC) and of the hardware implementation of its various functional blocks. Figure 3.12 gives a block diagram of the module.

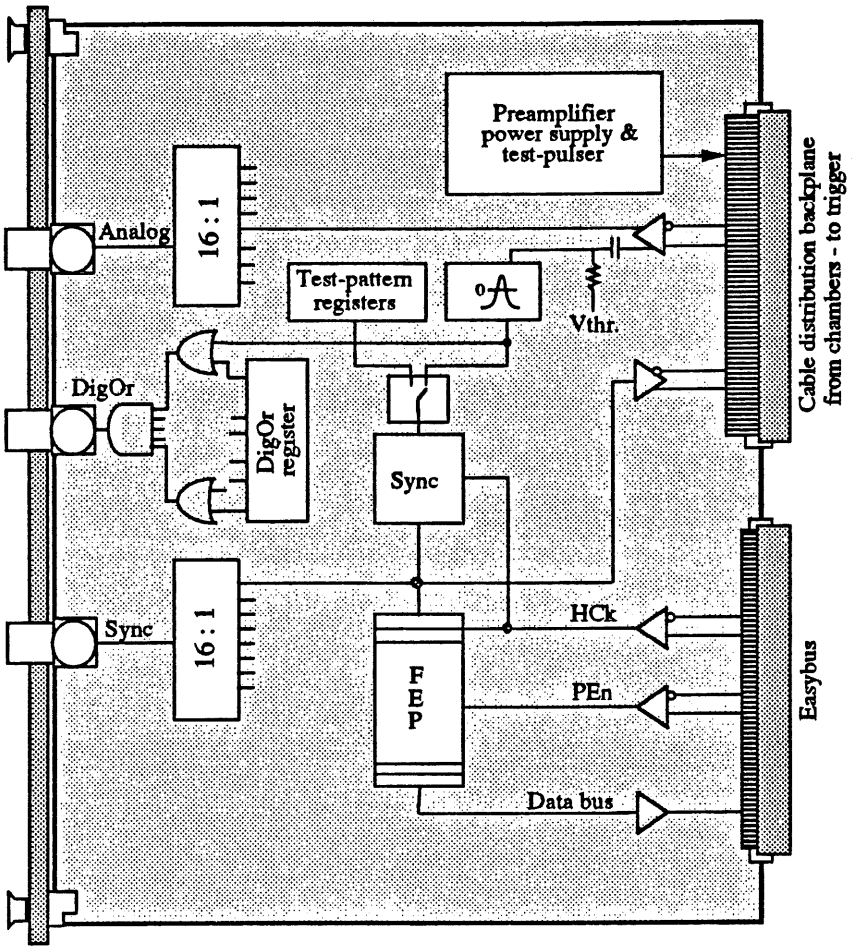


Figure 3.12: Schematic overview of the Receiver Card

3.6.1 General View

The Receiver Card [46] consists of a double-height, 220 mm deep, Euro module based on the user-defined Easybus backplane (see 4.5). The 50 Ω cable which leads the signals from the preamplifiers to the RC is brought to the rear of the module where it is plugged into a 5-row connector through a distribution backplane. After pulse shaping, the AC-coupled positive signal is summed to a negative DC threshold voltage and fed into a level-over-zero comparator. Each channel has an

individual threshold level adjustable in the range 0 - $\sim$ (−1 V). The second shaper output is connected through a 16-to-1 multiplexer to a front-panel connector for oscilloscopic observation of the analog pulses. The digital pulses at the output of the discriminator may also be monitored at the front edge of the cards through a 16-fold OR circuit with gated admission. This facility may be used, for instance, to measure counting rates or to drive a NIM trigger logic.

The discriminated signal is input into a gate array circuit which does the synchronization with the 10.4 MHz collider clock (HCk) and which contains the front-end digital pipeline (FEP). The input to this circuit may be switched from the chamber related signal to a test signal loaded by software in the "test-pattern registers". This connection allows to test the subsequent logics independently of the detector response and to replace defective or noisy channels by signals permanently on or off. After synchronization, the signal is input into the pipeline and distributed to the trigger electronics over a twisted-pair flat cable plugged in the rear connector. Again the possibility to observe the signal is provided. The data in the pipeline are read out over the local 16-bit wide data bus and the Easybus dataway located in the lower part of the card cage. This latter also distributes the HERA clock, the pipeline gate signal (PEn) and various local control lines to the RC. Finally, the RC supplies the necessary operating power to the preamplifier and sends test signals to them.

3.6.2 Threshold and Discriminator Circuitry

The DC level of the shaper signal at the OUTAC output is set by the threshold voltage applied on the INBIAS input of the shaper. The threshold voltage is supplied by the circuitry shown in figure 3.13. The 16 threshold values are stored in a 16-word × 8-bit RAM. The data presented at the output port of this memory control a multiplying digital-to-analog converter (DAC) with bipolar current outputs. An operational amplifier, connected in a transresistance configuration, is used to convert the DAC output current in a voltage $V_{thr} = -V_{ref}\ (N/256)$ where N is the digital input. In order to have the best resolution at low threshold values, a variable reference voltage V_{ref} is used. It is generated by a second op-amplifier with the non-inverting input maintained at a voltage $V_b \simeq 0.32\ V$ by a regulating diode. It follows that $V_{ref} = 3V_b/2 - V_{thr}/2$ and:

$$V_{thr} = \frac{-0.96N}{512 - N} \qquad 0 < N < 255 \qquad (3.16)$$

giving a step of 2.3 mV at $V_{thr} = -100$ mV and of 7.4 mV at the maximum value of $V_{thr} = -952$ mV. Figure 3.14 illustrates the function $V_{thr} = \mathrm{f}\,(\mathrm{N})$ as measured on a Receiver Card.

To save space and money, only one DAC is installed on each Receiver Card. A 4-bit counter, clocked by a 300 Hz oscillator, is used to present in a cyclic way the 16

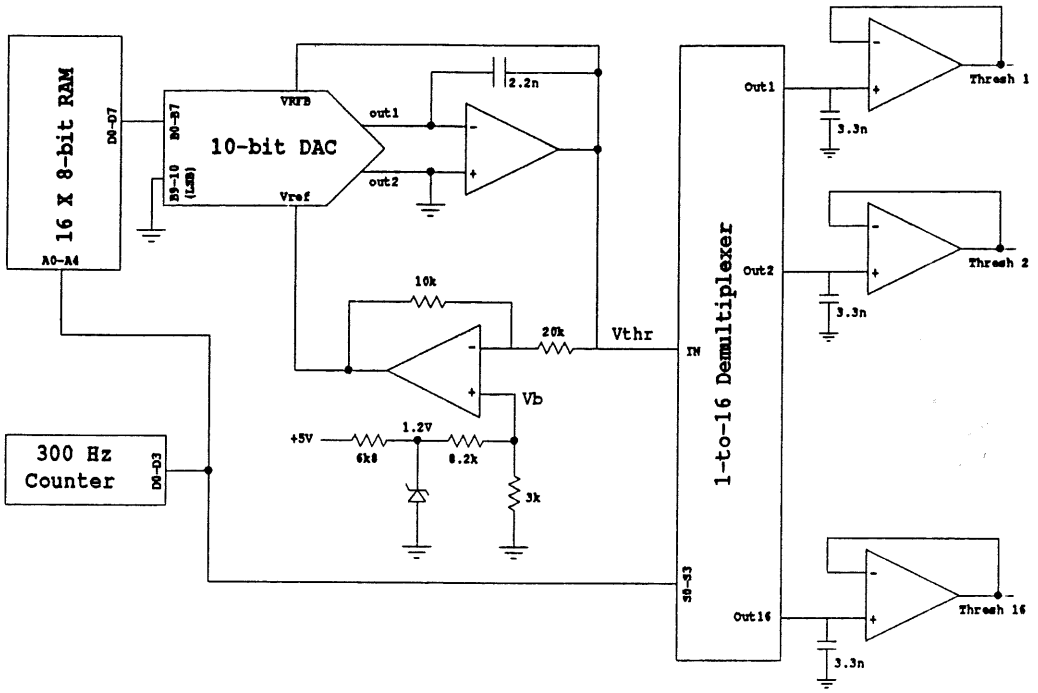


Figure 3.13: Threshold circuitry

digital threshold values to the input port of the DAC. The corresponding analog output is stored on a capacitor through an 1-to-16 demultiplexer driven by the same address as the RAM. The analog switch, the capacitor and the subsequent op-amplifier act as a sample/hold circuit. Through the cyclic operation of the counter, the 16 capacitors are continuously reloaded, minimising in this way the changes in the voltages due to leakage currents.

The negative threshold voltage is summed to the positive analog output of the shaper (see figure 3.15). The resulting signal is fed into the discriminator circuit which outputs a TTL signal with a width equal to the time over zero. The active circuit of the discriminator is a NE521 comparator. A positive feedback adds a small hysteresis (30 mV) which enhances the switching speed of the output transition and ensures that a noisy input is less likely to produce multiple triggering.

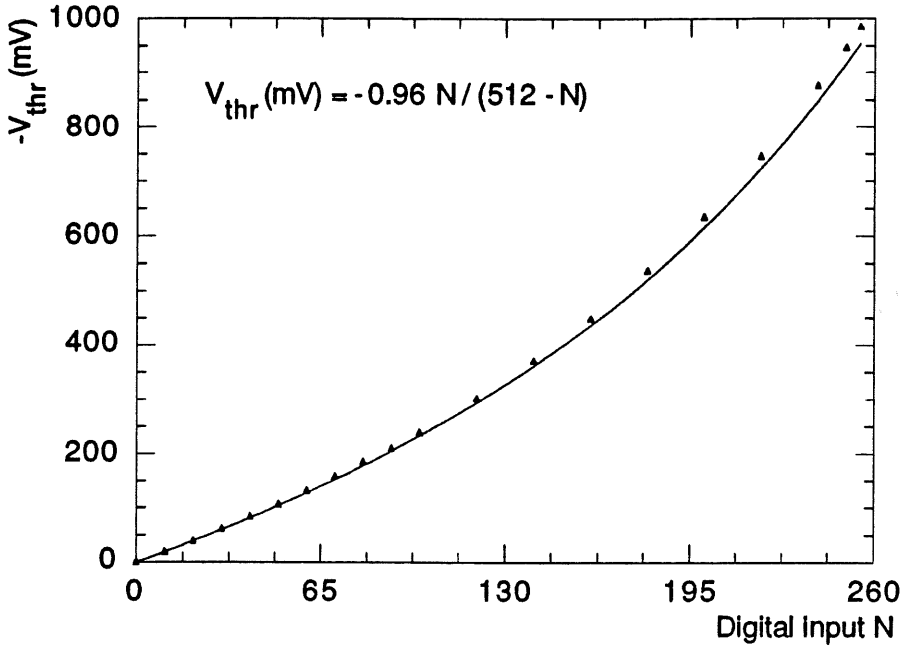


Figure 3.14: Threshold voltage vs digital input

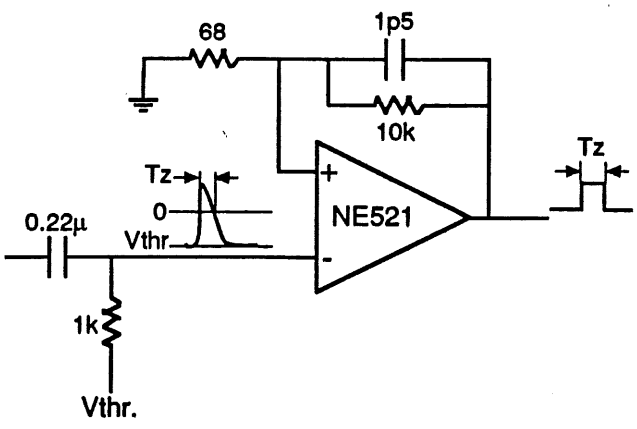


Figure 3.15: Discriminator

3.6.3 The Sync. Gate Array

The synchronizer circuit and the pipeline are part of a semi-custom integrated circuit designed in CMOS gate-array technology [47]. One 44 contact PLCC package contains the circuitry for eight channels. The Sync. Gate Array (abbr. Sync GA) has been originally developed for the readout of the muon iron instrumentation but other potential applications have been taken into account during its design. This section gives an overview of the Sync GA functions which are of interest in the MWPC context [48].

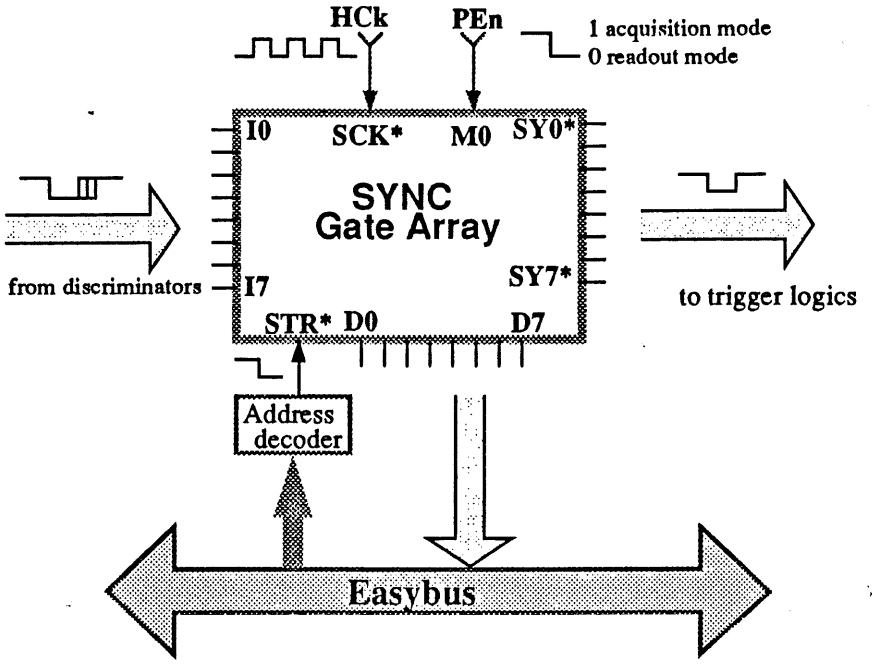


Figure 3.16: Bloc diagram of the Sync GA

Figure 3.16 shows a block diagram of the Sync GA implementation on the Receiver Card. The main connections to the circuits are :

In Asynchronous inputs into which the discriminated pulses are fed.

SYn* Outputs of the synchronizing circuit.

Dn* Outputs of the pipeline.

SCk* 10.4 MHz clock input.

M0 Mode control. Mode 0 is the readout mode (L1 not active), mode 1 is the acquisition mode (L1 active).

STR* A falling edge at this input advances the data in the pipeline during mode 0.

The input/output signal relation in acquisition mode is shown for a single channel in figure 3.17. If one or more falling edges occur at I within an interval

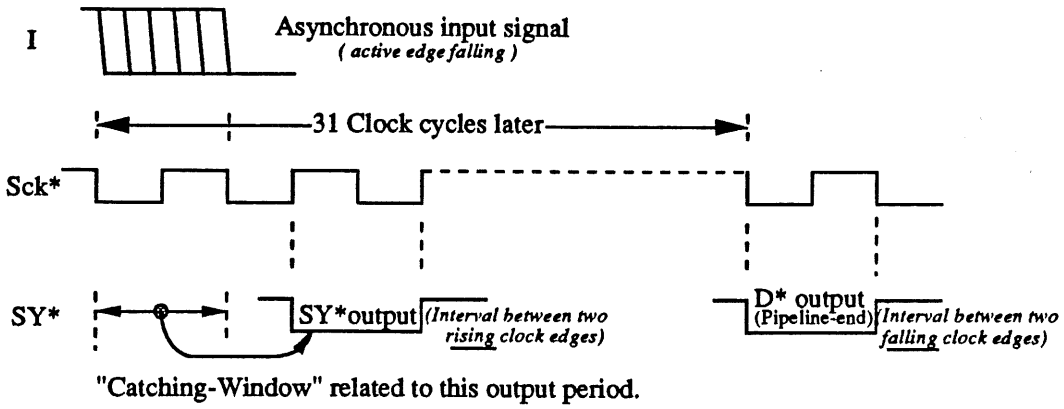


Figure 3.17: The Sync GA - Basic relations between input and output

(called "catching window") between two falling clock edges, then a low pulse will appear at the SY* output during the subsequent clock period between two rising edges. Thirty one clock cycles later this signal is presented at the D* output.

Let us now detail the synchronization part of the circuit shown in figure 3.18. In the initial state, all the flip-flops are in the reset condition (0 at the Q output) and a logical 1 is applied to the input I. If no edge arrives, the flip-flops stay in their 0-state, whereas a falling edge will set Q_{FF1} to 1. With the following SCk rising edge this 1 will be carried over into FF2 and the D-input of FF1 will be at logical 0. At the same time the output of the XOR gate goes to the high state. With the next SCk period, the Q-output of FF4 (SY*) is set to 0. If no further edges arrives at I, the second SCk falling edge will set Q_{FF3} to 1 and the output of the XOR gate goes to 0. The flip-flops FF4 is then reset on the next rising transition. If another pulse arrives at I at a later time, the same transitions are repeated with inverted polarity, except at the output of the XOR gate where a logical 1 will occur again for the duration of one SCk period. If a series of falling edges arrives at I during one SCk period, it leads to the same sequence as a single one. Because of internal propagation times, the catching-window differs from the ideal clock period. An intrinsic inaccuracy of maximum 11 ns has been measured, leaving 85 ns for all other jitter sources.

The output of the XOR gate is fed into the pipeline part of the gate array (see figure 3.19). This latter consists of a series of 30 flip-flops connected so that each Q output drives the next D input with all clock driven simultaneously. On each

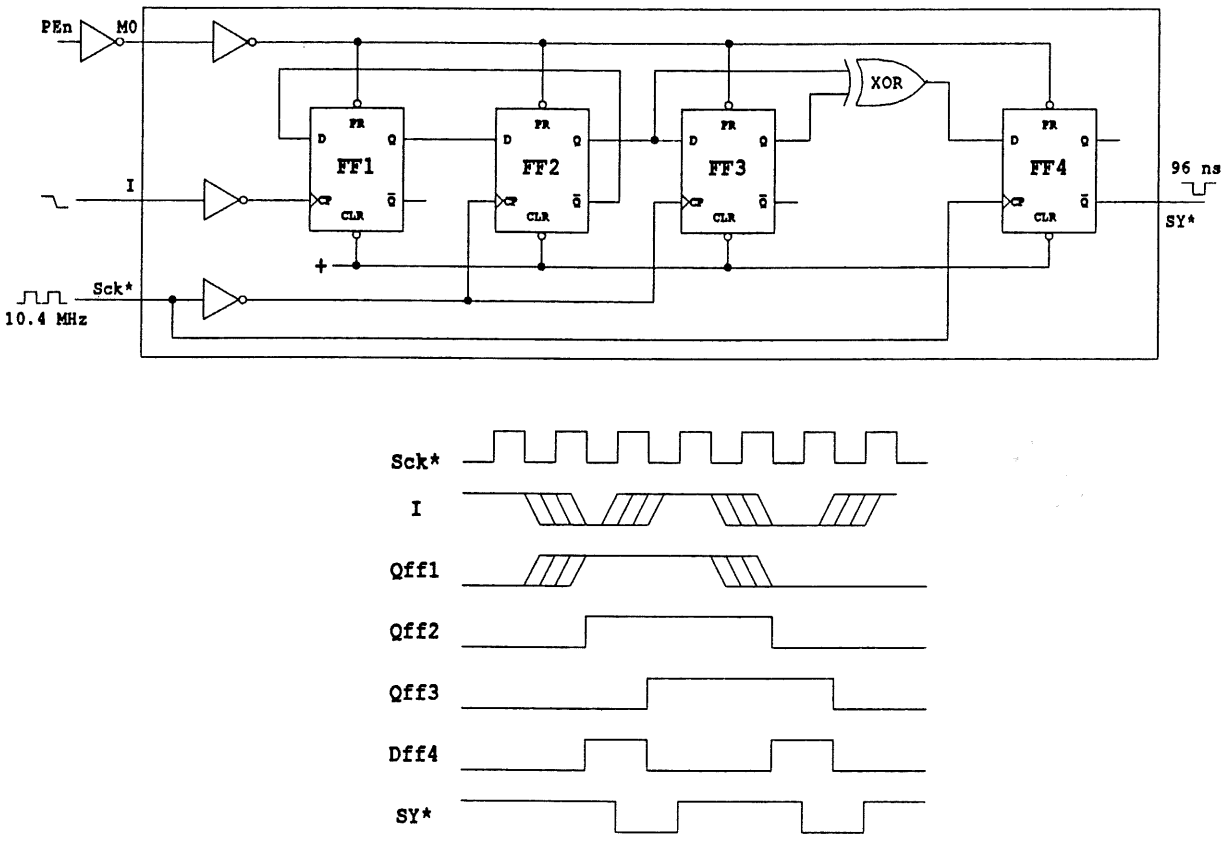


Figure 3.18: The Sync GA - Synchronization part

falling edge the pattern of 0's and 1's stored in the register shifts to the right, with the data at the first D input entering from the left. In this way, a signal at the input I will appear at the circuit output 31 clock cycles later. If an event candidate is detected, the Sync. GA toggles in the readout mode on the true-to-false transition of the PEn signal. The three flip-flops of the sync. circuit are then disabled, inhibiting entry of new data. If the event survives to the L2 trigger, the pipeline content is moved into the BDC FIFO buffers through the D port. This transfer is controlled by the STR input.

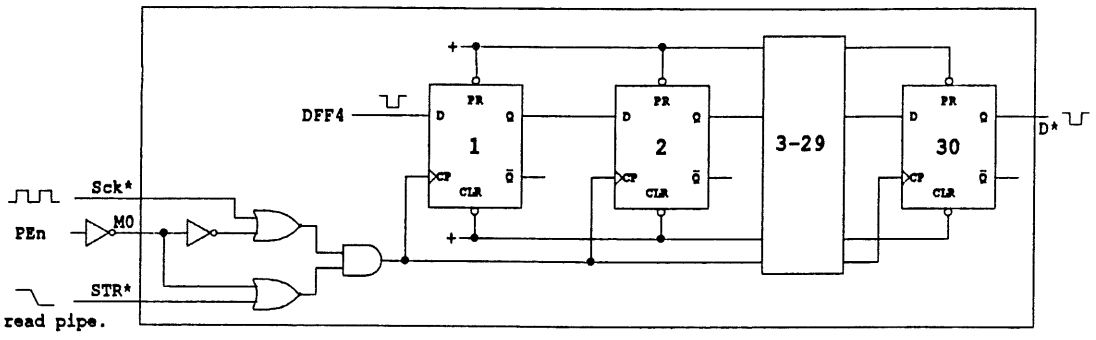


Figure 3.19: Sync GA - Pipeline part

3.6.4 Pattern Simulation

The input to the synchronization circuit may be switched from the discriminator output to a test-pattern circuit. This facility has various applications:

- Surpass noisy channels or set to active defective channels depending on what is most favourable to the subsequent trigger logic.

- Mask the channels which are not connected and thus have an open shaper input . For instance, for the COP detector only 12 channels out of the 16 channels per Receiver Card are connected to the chamber. By presetting to zero the input to the synchronization circuit, these 4 unconnected channels appear as "zero signal" channels in the zero-suppression algorithm adapted for a 16 channel/Receiver Card configuration.

- Generate predefined sequences of signals into the pipeline and the trigger electronics in order to test the readout chain and the performance of the trigger logic.

- Load the various configuration registers of the ray finder gate arrays in the Z-vertex trigger electronics during the initiation phase of the system.

In fact, two test bits can be stored for each channel. An external signal broadcast by the STC (see 4.6.4) controls which one is fed into the sync. gate array. This allows to send to the trigger electronics and into the pipeline a predefined sequence of 0's and 1's.

3.6.5 The Monitoring Circuits

3.6.5.1 Analog Monitoring

The analog pulses at the shaper DC outputs are multiplexed to a common LEMO output on the front panel of the module. This allows external observation of the pulse shape and various analog measurements, e.g. pulse height spectrum recording.

3.6.5.2 Digital Monitoring

The unsynchronized digital signals are fed into a 16-fold logical OR output of which is available as well on the front panel as on the rear 4-row connector. Two LEDs connected to the output of the overall ORs of the ch. 0-7 and ch. 8-15 are added for quick visual rate check. The admission of each channel to the OR circuit is gated by a software-controlled bit which allows to select appropriate patterns of channels. This circuit can serve different purposes:

- Measurement of the counting rate of single or multiple channels.
- Measurement of the time distribution of the signals respective to the HERA clock.
- Input to a trigger logic based on the sector segmentation of the chambers, e.g. cosmic ray trigger.

After their synchronization with the collider clock, the signals can be again monitored through a 16-to-1 multiplexer. An output is also provided to measure the phase adjustment of the HCk signal in the crate.

3.6.5.3 Voltage Measurements

Various analog voltages and currents on the Receiver Card can be measured by the ADC on the Controller Card through the Easybus analog lines. This feature is essentially used to check the status of the front-end electronics before starting a new data taking session. The following measurements can be done :

- threshold voltages.
- preamplifier supply voltages on the detector and at the near end of the cable for detecting abnormal drops.

- preamplifier supply currents.
- voltage difference between the local and the preamplifier ground levels.
- regulating diode voltages.

Chapter 4

Implementation of the MWPC Readout System

4.1 Introduction

The MWPC data pipelined on the Receiver Cards are readout in an independent branch of the H1 data acquisition system. This branch is also responsible for the data acquisition of the TOF counters and the readout of the MWPC trigger decision data. In total, about 6 kbytes[1] of raw digitised information per event need to be transferred, compressed and assembled as event records in the MWPC multi-event buffer. In addition to this, tools for monitoring and testing the hardware and software functions must be provided.

This chapter describes the way in which these tasks are executed in the MWPC branch with emphasis rather on the hardware implementation than on the software development. An overview of the constituent elements of the readout chain is presented first, followed by a description of the data flow. Next, the hardware components are detailed, in particular the modules which have been specially developed for the MWPC readout. This is followed by the description of the synchronization mechanisms. Finally the performance of the system is discussed.

4.2 System Overview

The MWPC readout system is schematically represented in figure 4.1. It consists of 4 parts : the front-end electronics (MWPC and TOF Receiver Cards, trigger

[1] If not stated otherwise, the numbers given in this chapter corresponds to a configuration where the data from 10 time slices are readout for each triggered event.

systems), the local Master Crate, the Subsystem Trigger Controller and the on-line monitoring system.

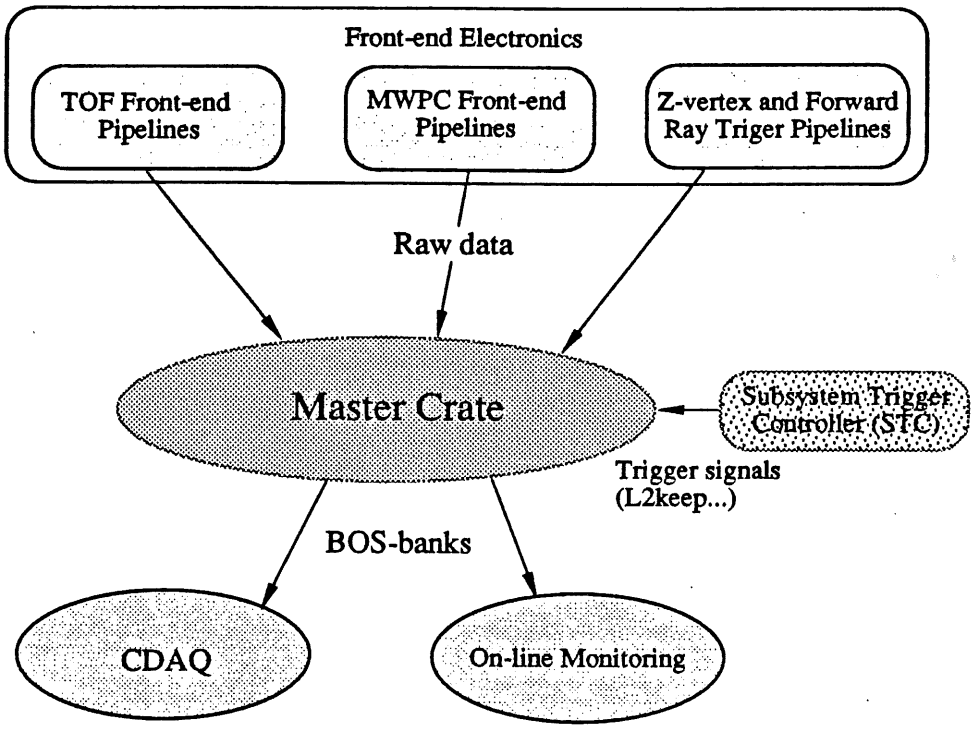


Figure 4.1: MWPC readout system

4.2.1 The Front-end Electronics

At the lowest level of the readout chain reside the front-end (FE) electronic modules equipped with shift register pipelines in which data are stored during the level 1 and level 2 trigger decision times. The front-end consists essentially of 264 Receiver Cards used to process the signals from the multiwire proportional chambers as described in chapter 3. The signals from the TOF scintillators are discriminated and synchronized in a separate NIM hardware set-up . To include the TOF data hits in an event record, the outputs of the NIM synchronizer elements are connected to 5 additional Receiver Cards specially adapted to receive NIM signals. The decision data from the Z-vertex (ZVTX) and forward ray finder (FWRF) trigger systems are stored into memories which are read in the same way as the Receiver Card pipelines.

The three front-end parts are distributed between 25 Euro-crates equipped with a special bus,the "Easybus", which is essentially a simplified 16-bit wide VMEbus with additional analog and ECL signal lines. The crates are grouped into 6 readout

branches linked to the Master Crate by vertical cable busses (figure 4.2). Data

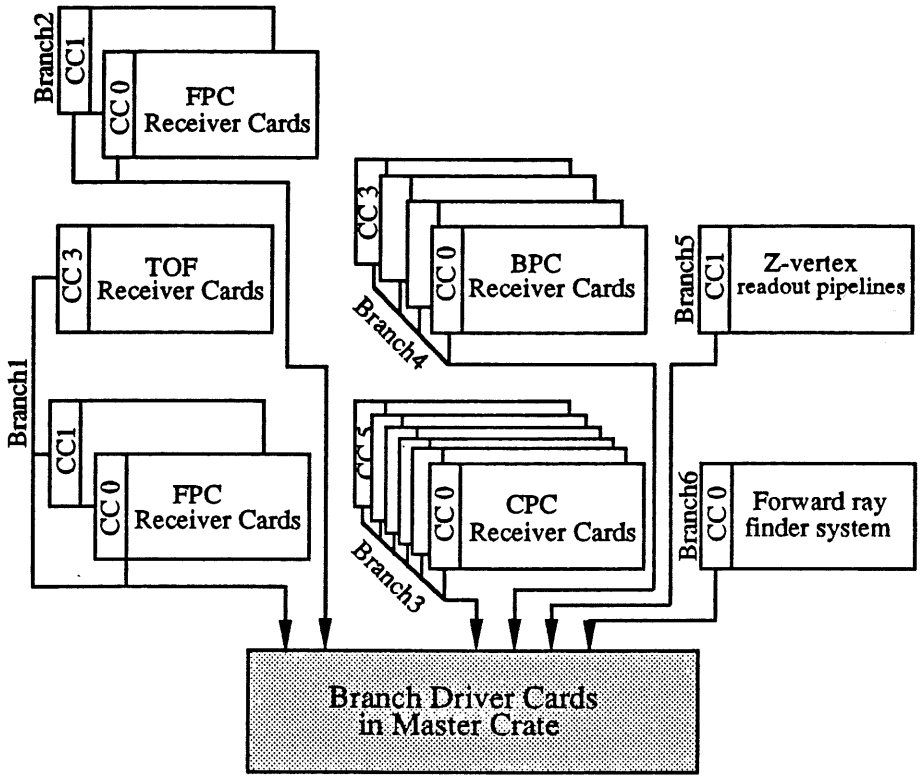


Figure 4.2: Front-end crate configuration (only the readout connections are shown)

transfers are controlled in each branch by a Branch Driver Card (BDC) residing in the VME Master Crate and by a Controller Card (CC) in each FE crate.

In each branch, the FE crates are organised in such a way that they can be accessed in pairs, or "units", allowing a 32-bit transfer format for the data acquisition. In addition, the BDC is equipped with a DMA controller that allows front-end data to be moved into a 4k deep FIFO buffer residing in the BDC without processor intervention. Table 4.1 summarises the distribution of the FE crates over the 6 branches.

4.2.2 The Master Crate

The Master Crate is the coordinating core of the MWPC readout system. It contains the supervisor readout controller and allows data exchanges between the different parts of the system and with external computers. Figure 4.3 shows the

Branch	*Front-end crates*	*CC (unit)*	*♯ modules*
1	FPC Receiver Cards	0 (0)	12
	" "	1 (0)	20
	TOF Receiver Cards	3 (1)	5
2	FPC Receiver Cards	0 (0)	20
		1 (0)	20
3	CPC Receiver Cards	0 (0)	16
		1 (0)	16
		2 (1)	20
		3 (1)	20
		4 (2)	20
		5 (2)	20
4	BPC Receiver Cards	0 (0)	20
		1 (0)	20
		2 (1)	20
		3 (1)	20
5	Z-vertex finder and RAM Cards	1 (0)	20
6	Forward ray finder system	0 (0)	20

Table 4.1: Distribution of the front-end crates

configuration of the crate. The readout controller (2)[2] is a 68030 processor based computer board. It is responsible for the hardware initialisation and manages all real-time tasks during data acquisition. Program and data storage is provided by on-board static RAM with external access through the VMEbus port. The program code and a default data-base describing the system configuration reside permanently on a separate 512 kbyte EEPROM memory board (9). This allows an automatic start-up of the DAQ program without operator intervention after a power-cut. User settings (thresholds, test-patterns...) are loaded in a 1 Mbyte SRAM bank on the same board.

The Master Crate is linked to the front-end electronics via BDC modules (10-15) as described above. The connections with the Subsystem Trigger Controller and the monitoring system are performed by two interface boards : a VMIC VME extender (17) and a VICbus controller (8) respectively. A VMEtaxi (4) connects the MWPC system to the H1 central data acquisition via an optical fibre link and serial lines. Information and data are exchanged between the two systems via the multi-event buffer (5), a dual-ported VME-VSB 512 kbyte static RAM. The MEB is addressed by the CDAQ over a VSBbus to leave the VMEbus free for the front-end data acquisition.

[2]In this section and in 4.2.4, numbers between brackets refer to the position of the boards in the crate.

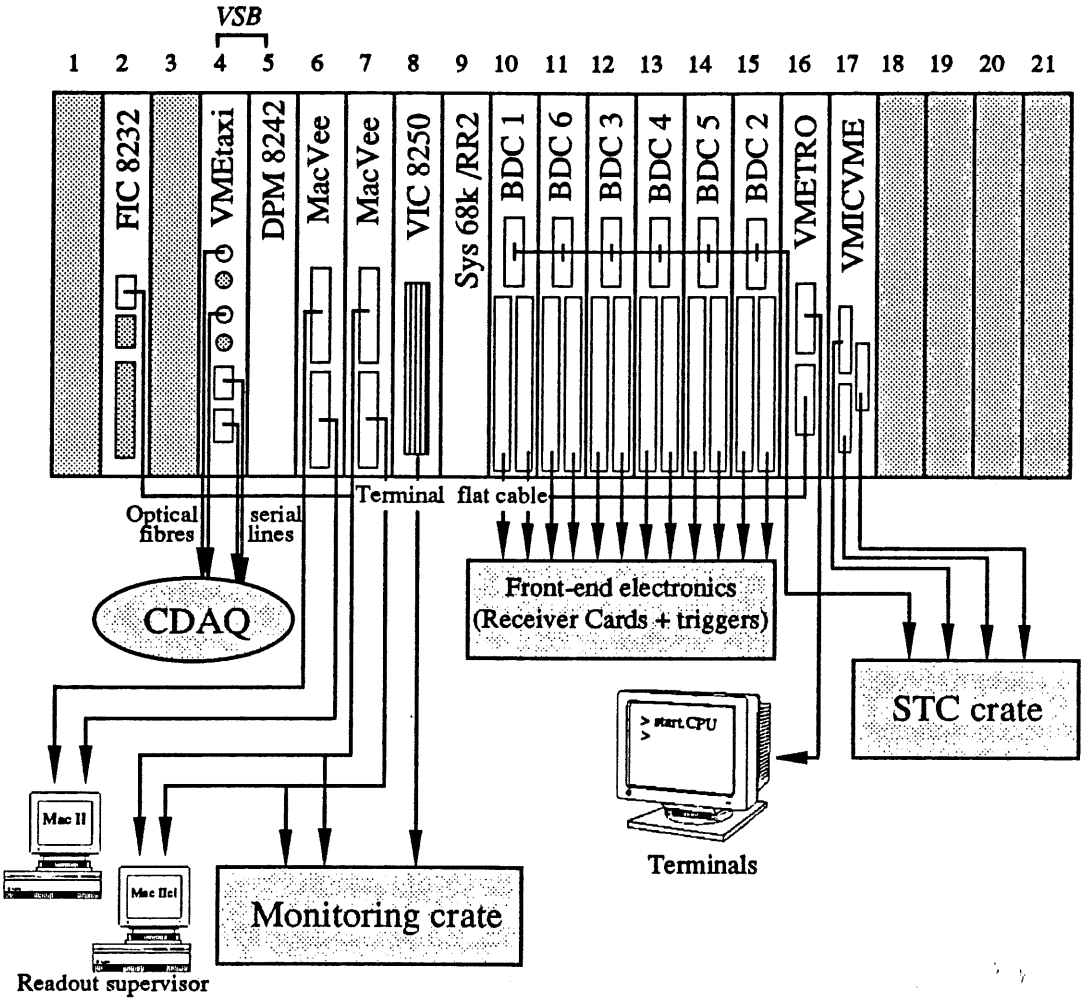


Figure 4.3: Master Crate configuration

All VME modules in the system may be accessed from two MacII computers connected to the Master Crate by MICRON-MacVee interfaces (6, 7). A terminal allows to access the readout controller through its serial interface. It serves also as display for the VMETRO module (16), a debugging tool used to monitor the VME activity.

4.2.3 The Subsystem Trigger Controller

The Subsystem Trigger Controller (STC) is the interface between the Central Trigger Controller (CTC) and the MWPC readout system. It contains a set of control modules which coordinate the readout sequence with the trigger signals and broadcast information from the HERA machine and the trigger processors. The

STC communicates with the readout controller through VMEbus read-write cycles and interrupts. Multiple signal ports are provided to distribute control signals to the front-end electronics. All time critical signals are transmitted over twisted-pair cables through fanout ports with adjustable delays. This allows precise timing of the active signal transition with respect to the HERA bunch clock.

4.2.4 The Monitoring System

The monitoring system provides an on-line check of the chamber performances and of the operation of the front-end and trigger electronics. It is housed in a separate crate in order to decouple the readout and monitoring related data transfers. Figure 4.4 shows its configuration.

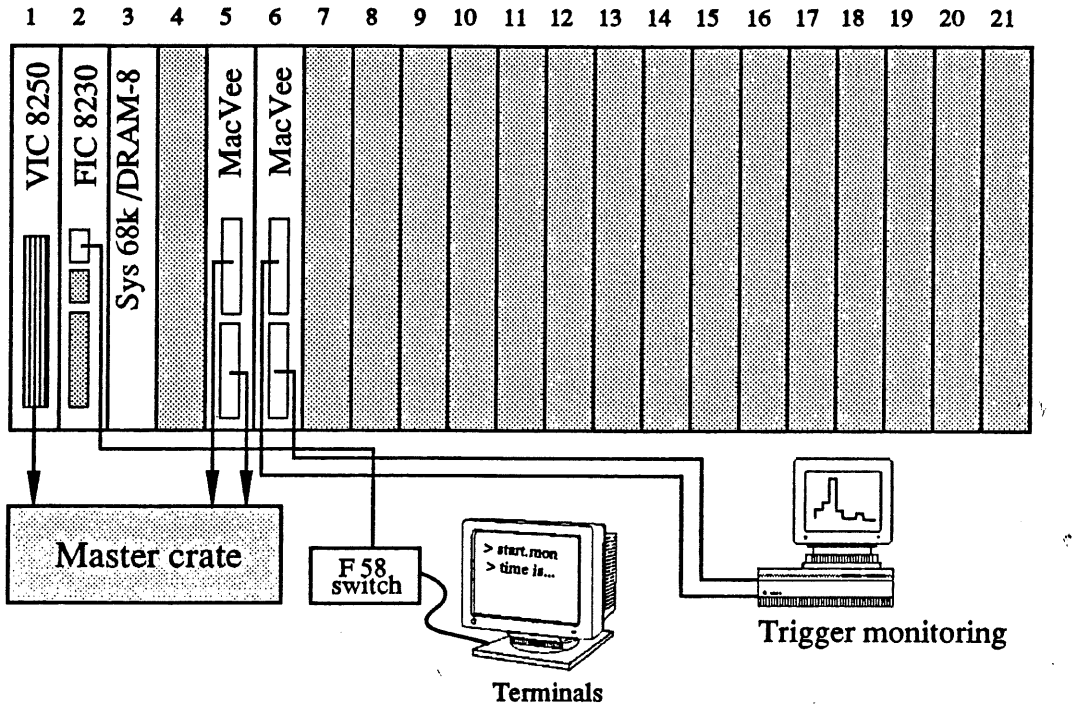


Figure 4.4: Monitoring harware set-up

The monitoring of the detector data is done by a VME 68020 processor board (2) combined with the supervising MACII computer. On the former, events are gathered, analysed and checked with high speed. Interesting parameters for monitoring are accumulated into 1 or 2 dimensional histograms. The software code originates off-line and is written in Fortran. A 8 Mbyte memory board (3) is used as working space for histogramming and to store large data-bases. The MACII computer is connected to the VMEbus via a MICRON/MacVee interface (5). A

protocol between the VME processor and the MACII was developed which allows to control the monitoring process. Stored monitoring data can be retrieved on request and analysed using the graphical interface of the MACII.

The monitoring of the trigger decision data is performed on a second MACII connected via an additional MacVee board (6) in the monitoring crate. Trigger data are directly gathered in the computer memory and analysed without processing in the monitoring crate.

4.3 Data Flow

The data flow through the MWPC readout system is schematically represented in figure 4.5. The readout procedure includes two asynchronous steps : the front-end freeing and the front-end event building.

4.3.1 Front-end Freeing

On an accept signal from the second level trigger, the DMA controllers on the BDCs automatically start the readout of all pipeline memories. The data from a programmable number (Nbc) of consecutive registers, centered around the register containing the data which triggered the system (bc 22,cf. 3.4), are transferred over the vertical bus in the FIFO buffers. These buffers can accumulate several events. Simultaneously, the readout controller reads scaler information in the STC including the event number. Since the STC has no buffering capabilities, these data are buffered in the FIC memory.

In parallel with the front-end readout, the L3 processors prepare the third level trigger decision(cf. 2.3.4). A L3keep signal is used as a flag to indicate that the event has to be passed to the next stage of the acquisition. On the other hand, if the event does not satisfy the trigger conditions (L3reject), the front-end readout is immediately aborted without processor intervention. The state of the transfer counters in the DMA controllers is then recorded to determine the amount of L3reject related data already transferred in the FIFO buffers. Once this is done and all FIFOs can hold a complete new event, the readout controller signals to the CTC that the system is ready to accept a new L2keep. When no new event can be stored in the buffer the ready signal is postponed until enough space becomes available.

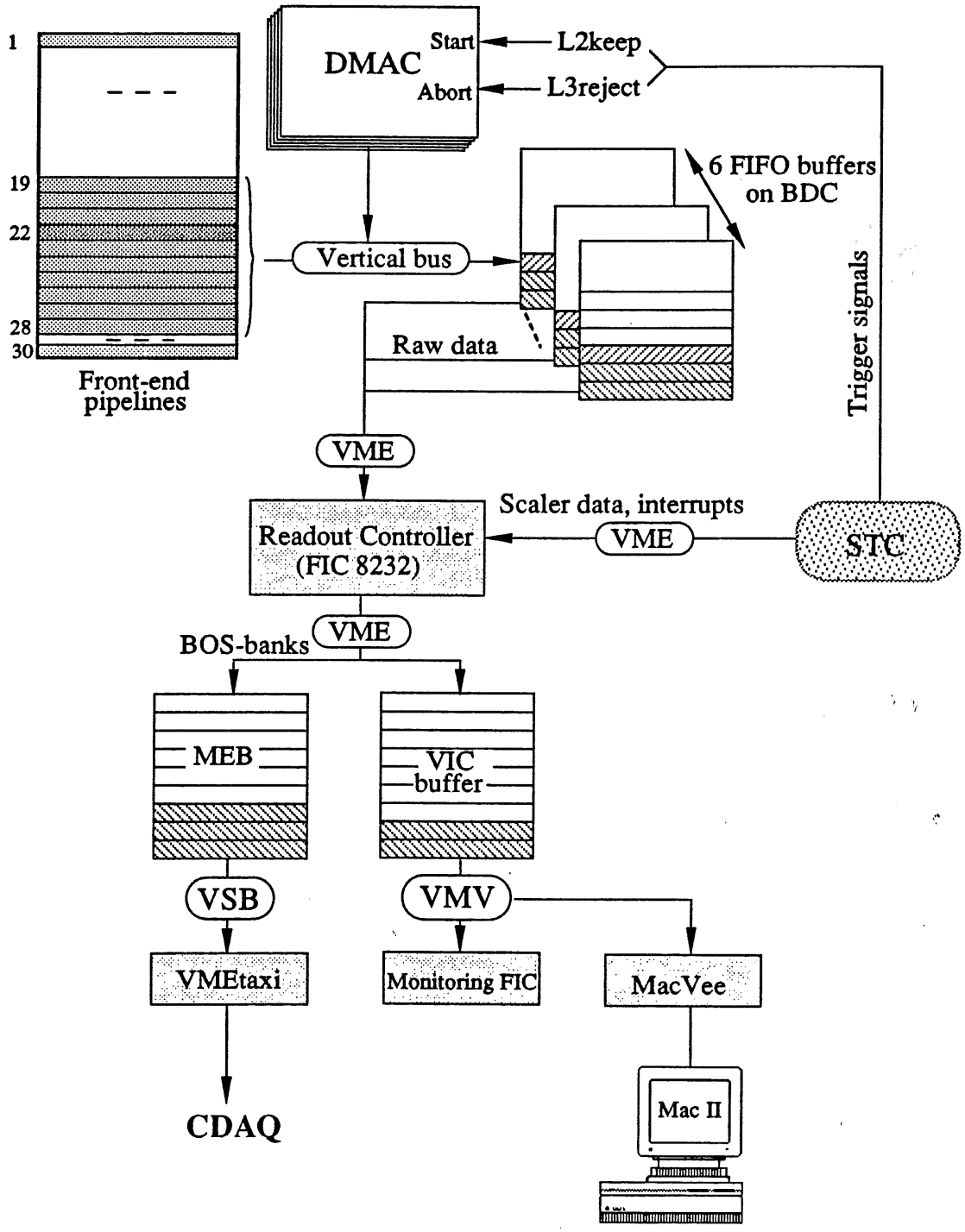


Figure 4.5: Data flow through the MWPC readout system

4.3.2 Front-end Event Building

The data stored in the FIFO buffers are read by the readout controller over the VMEbus and formatted into the MEB asynchronously to the front-end transfer. Since there is buffering, it is possible that the event which is prepared for CDAQ is not the most recent one. However the events are treated sequentially in strict event order. If the queue in the FIFO is empty when a new front-end transfer is initiated, the controller starts to treat the new data as soon as a BDC signals that they are available, even if the L3 decision is not yet made. The data are assembled into the MEB as a complete event record with the proper format. In short, a zero-suppression algorithm is applied to the MWPC and TOF data and for every detector and time slice a BOS-bank is created, consisting of the formatted data plus a header record identifying the contents of the information. Additional BOS-banks are written with time and counter information from the STC and data from the ZVTX and FWRF systems.

When a L3keep associated event is ready in the MEB, the CDAQ event coordinator is informed that valid data are available. The event coordinator will read the MWPC banks together with the other subdetector data to form a full-event record when it is free to build a new event. In case a L3reject is sensed, the buffer space associated with this event in the MEB is kept for the next event and data still in the FIFO buffers are flushed hardware upon a software command. Each time the readout of a new event is started, the controller checks whether a monitoring task posted a request for data. If so, an additional copy of the data in the MEB is written in the internal buffer of the VIC board. These data are complemented with the non zero-suppressed bit patterns and some status information such as the trigger rates and dead time estimates.

Whereas the time scale for the front-end transfer is of the order of a few hundreds of microseconds, the data collection into the MEB may require several milliseconds. Events for which monitoring data are requested can increase up to 50% this time, depending on the amount of non-zero data. However, as long as no FIFO buffer is saturated, dead time occurs only during the front-end freeing. When a FIFO cannot hold a complete new event, additional dead time is generated until the oldest event in the buffers has been completely treated. The running conditions which can lead to such a saturation state are discussed in 4.9.

4.4 The Branch Driver Card

4.4.1 Introduction

The Branch Driver Card (BDC) performs the connection between the MWPC master crate and the vertical bus. It consists of a double height VME slave module which acts as a branch driver for a maximum of 8 Easybus crates.

The first function of the BDC is to allow modules in the Easybus crates to appear within the address space of the VMEbus. The BDC decodes the VME data transfer cycles and performs automatically the required operations on the vertical bus, so that the interface is transparent to the user. Data transfers in 32-bit format are fully supported by combining two Easybus crates.

The second function of the BDC is to provide a block transfer facility coupled to a dual-ported buffer and a zero-wait state memory. This mode is intended for sustaining high speed block transfers between the Easybus crates and the data buffer during the data acquisition sequences. In the design of the vertical bus, special emphasis has been placed on the optimization of the bandwidth. Particularly, the 32-bit format allows to operate in parallel the readout of two front-end crates.

This section provides an overview of the hardware architecture and the operating principles of the BDC. For a detailed description, refer to the BDC user's manual [49].

4.4.2 Block Diagram Description

The BDC module can be regarded as consisting of several functional blocks, as shown in figure 4.6 :

- the VME slave interface which connects the module to the VME dataway.
- the vertical bus master interface which controls the data transfer with the Easybus crates.
- the STC interface which allows to communicate with the MWPC Sub-Trigger Controller.
- the local resources (DMAC, SRAM, input FIFO).
- the global resources (status and control registers, output FIFO).

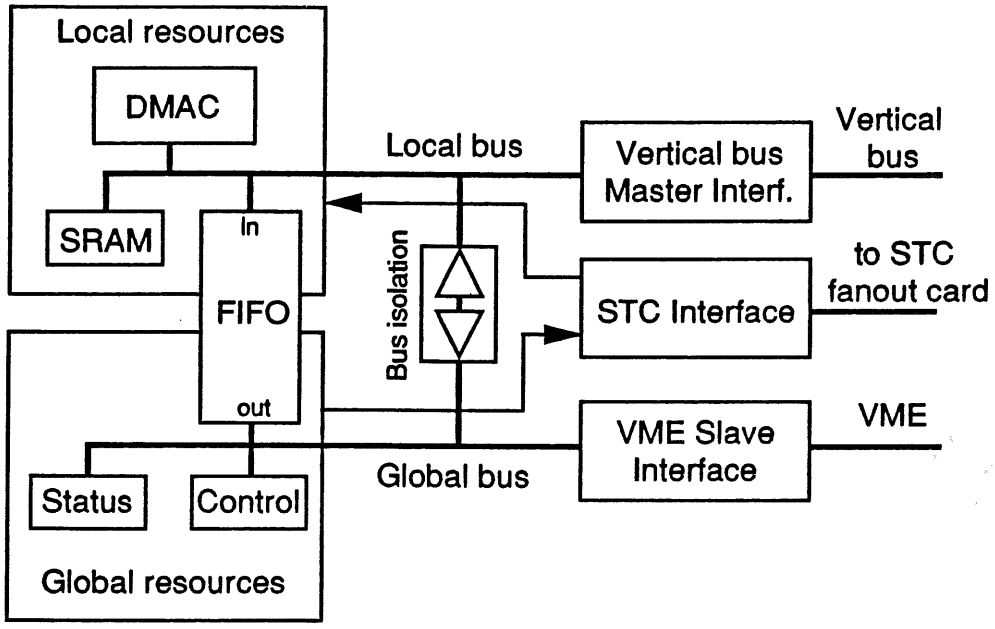


Figure 4.6: BDC block diagram

These blocks are interconnected by two internal busses :

- local bus, A19 : D32.
- global bus, A18 : D32.

The heart of the module is the direct memory access controller (DMAC). It can perform data block transfers between the memory locations attached to the local and vertical busses. During data acquisition sequences, the data are read by the DMAC from the front-end electronics over the vertical and local buses and are written into the high speed FIFO buffer. Up to 4 K × 32-bit data can be stored locally. The data are transferred over the VME using a separate output port on the global bus controlled by the readout controller. During the DMA transfer, the two BDC busses are electrically isolated. This structure allows the VME data transfer to run asynchronously from the front-end data acquisition without any bus arbitration time overhead.

The DMAC operates in a mode using a descriptor list to steer the data acquisition transfer. This list is loaded in the local static memory (SRAM) and contains the base address and the size of all the data blocks to transfer. The basic DMAC operations, e.g. transfer request and abort, are controlled either by means of VME commands or by external signals through the STC interface. To inform the readout controller of events, the DMA controller can generate VME interrupts.

When the DMAC is not active, the local and vertical busses can be directly accessed from the VME dataway. The resources attached on these busses are then mapped in an 1 Mbyte window of the 4 Gbyte VME extended address space. This allows a VME processor to control directly the settings of the DMAC and of the front-end electronics during the initialization phase of the readout process. On the other hand, the global resources are always accessible from the VME port even during DMA transfers. In particular, the status and control registers are used to determine the current status of several on-board devices and allow to modify certain module operations.

4.4.3 The Bus Interfaces

4.4.3.1 The VME Slave Interface

The VME slave interface contains the backplane bus interface logic. The main element is the address decoder which maps the BDC resources and the vertical bus in an 1 Mbyte window of the VME extended addressing space. In this window, the front-end crate address decoding is organized in order to support data transfers in 32-bit format. This is achieved by combining two 16-bit crates into the same 32-bit memory area (see figure 4.7). The memory is organized on a word-addressable basis where lower addresses correspond to higher order words (M68000 convention). The address N of a longword datum corresponds to the address of the most significant word. The lower order word is located at address N + 2. A crate corresponding to the least (most) significant word is called 'down' ('up'). Two crates which are mapped together are in the same 'unit'.

4.4.3.2 The Vertical Bus Master Interface

The vertical bus master interface transmits the VME or DMAC cycles to the vertical bus. The transfers are performed with an asynchronous bus protocol over a non-multiplexed 19-bit address and 32-bit data bus. The signals are distributed in differential form to assure a good noise immunity. The physical connection between a BDC and the front-end crates is made by two 60-conductor twisted pair cables plugged into front-panel connectors.

4.4.3.3 The STC interface

The STC interface receives from the subsytem trigger controller the transfer request and abort signals which control the operation of the DMAC. To the STC, it drives two signals which reflect the status of one control register bit and of the

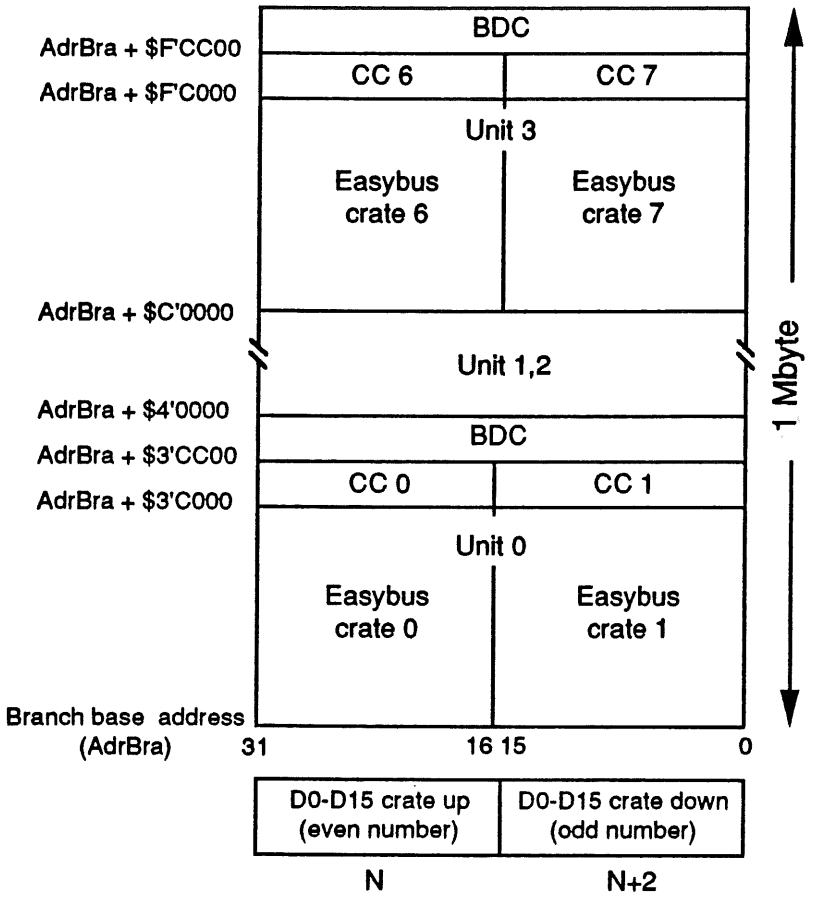


Figure 4.7: Data organization in a branch

FIFO read pointer. The connection between the two systems is made by a 2 × 10-pole flat cable plugged into the BDC STC front panel connector and a Fanout Card output port.

4.4.4 The Static RAM Memory

The BDC contains a high speed SRAM offering no wait state for DMAC access cycles. The memory area is made by two 2K × 8-bit RAM devices. It is used to store the block descriptor array when the DMAC operates in chaining mode.

4.4.5 The FIFO Buffer

A communication memory, with two separate read and write ports, and working in the first-in first-out (FIFO) mode, is implemented between the local and global

resources. The organization of the memory allows a 4096 deep 32-bit wide buffer structure. Two bits in the status register provide the status of the queue in the FIFO. The Empty flag is asserted to zero when all data have been read from the queue, inhibiting any further read access. The Full flag is set to zero when there are no more empty locations in the memory array, inhibiting further write transfers. The FIFO also features a "fast flush" facility which allows to increment at a high rate (20 MHz) the read pointer by an offset. This mode is intended for flushing the L3reject events with minimal intervention from the system processor.

4.4.6 The DMA Controller

To operate the data transfers from the front-end pipelines into the local FIFO buffer, a direct memory access controller (DMAC) is implemented on the BDC. The advantages of this configuration are twofold :

- The operations that occur on each data transfer, such as counting the number of words, sequentially incrementing the memory address and checking whether the required number of words in a block has already been transferred, are performed by hardwired logic rather than by CPU instructions. Hence the data block transfer speed is only limited by the memory cycle time.

- The basic transfer functions of a DMAC can be directly controlled by external signals. So data transfers may be started or aborted at any time without the usual time overhead of program controlled interrupt sequences.

On the BDC, the MC68450 DMA controller has been selected. The manner in which this device handles data transfers is briefly described below. A complete description of the MC68450 controller can be found in the manufacturer's data sheet [50] and in the BDC user's manual [49].

Figure 4.8 illustrates the block transfer configuration. Any transfer cycle follows the same basic steps :

1. Channel initialisation

   During this phase, the readout controller loads the internal registers of the DMAC with control information, address pointers and transfer counts. The controller contains 4 independent channels but only one is used to operate the transfers. The initialisation ends by starting the active channel. The DMAC is then waiting for a transfer request.

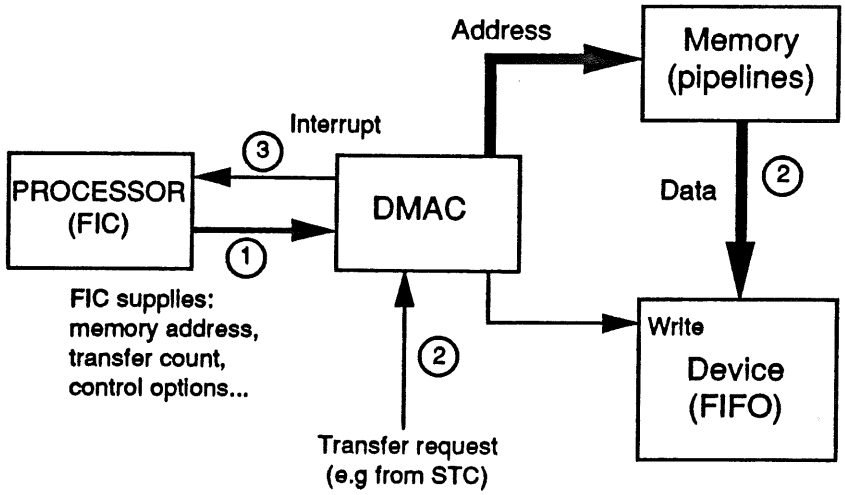


Figure 4.8: DMAC configuration

2. Transfer phase

During the transfer phase, the DMAC accepts a request for data transfers (L2keep signal) and provides addressing and bus control to access the Receiver Card pipelines. The FIFO is implicitly addressed by the controller using a handshake signal. In this way, the data are moved directly into the FIFO in one bus cycle. This protocol allows data movement at rates approaching the bandwidth limit of the Easybus, typically 4.5 Mbytes/s.

3. Termination phase

The termination phase occurs either after the normal completion of the transfer or the occurrence of an exceptional condition (transfer abort on L3reject or error). In both cases the DMAC generates a VME interrupt request to inform the event builder of its status. In response, the processor executes an interrupt acknowledge bus cycle and reads a vector number to identify the interrupt source. In case of a normal transfer completion or a L3reject, the readout controller executes an appropriate termination sequence in order to restore the DMAC registers in their initial state. The controller is then ready for a new cycle. If an error interrupt vector is returned, the program is aborted without any recovery attempt.

To minimise the time required to perform the zero-suppression, data corresponding to a specific time slice must be buffered in a contiguous block into the FIFO. This requires to read sequentially the data word corresponding to the same bunch crossing in all front-end pipelines and to repeat this operation for all the slices to read out. Unfortunately the pipeline addresses

are not contiguous in the DMAC memory mapping. To overcome this problem, a programmable memory management unit has been implemented on the BDC. This device translates in $\sim$ 25 ns logical addresses driven by the DMAC into physical addresses. In each branch a specific translation algorithm is implemented that groups the addresses of all the pipelines located in the same crate or unit. Furthermore, the DMAC operates in the "sequential array chaining" mode which allows to transfer in a single channel operation several non-contiguous data blocks. In this way, the full bandwidth of the DMAC can be exploited while structuring correctly the data in the FIFO buffer.

4.5 The Controller Card

4.5.1 General Description

A block diagram of the Controller Card (CC) is shown in figure 4.9. The pri-

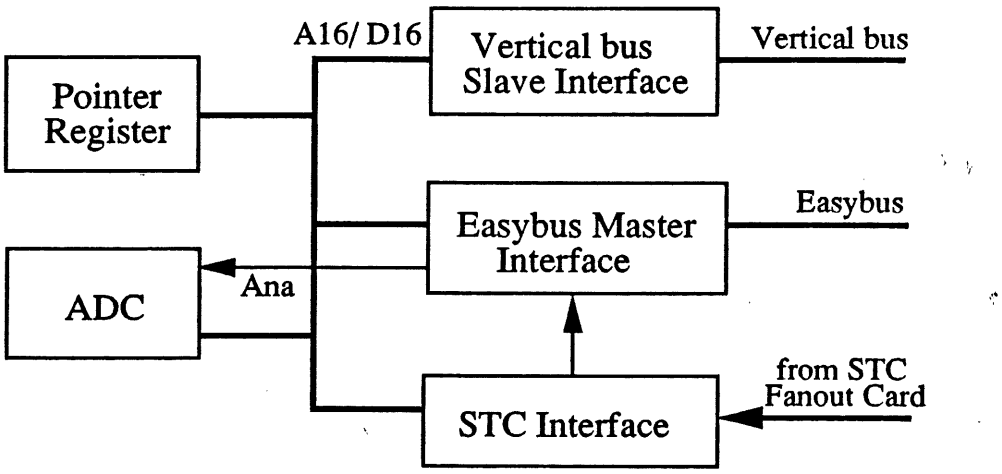


Figure 4.9: Controller Card block diagram

mary function of the module is to convert vertical bus into Easybus cycles. The Controller Card automatically transforms the VMEbus and DMAC data transfer cycles into Easybus operations so that the interface is transparent to the user. The CC contains also a signal port which transceives signals from the STC to the Easybus backplane. These signals drive on the Receiver Cards the following circuits : the synchronization-pipeline gate array, the test-pattern circuitry and the test-pulse generator. An analog-to-digital converter on the CC allows to measure analog voltages (e.g. threshold levels) on two dedicated backplane lines driven by

the Receiver Cards. In addition a 16-bit register is available which allows to test the vertical connection.

4.5.2 Data Transfer and Easybus

The data transfer protocol on the vertical bus is asynchronous as on the VMEbus. Two handshaking lines work as wait signals between the Master Crate and the Easybus slave crates. These signals are generated either by 2 Controllers separately during a 32-bit transfer or by a single module during a 16-bit cycle. Two data strobes, generated by the branch driver, determine the data transfer format. They control a 32-bit data multiplexer which connects the Easybus dataway to either the lower word ($D_0 - D_{15}$) or the upper word ($D_{16} - D_{31}$) of the vertical bus. The addressing range of a Controller is decoded by the module number set on the front-panel rotary switch. After the address decoding phase, the Controller Card issues a data transfer cycle over the Easybus or internally to a local resource.

The Easybus is an user-defined 16-bit backplane bus originally conceived to connect the Receiver Cards to the MWPC readout system. Basically, it uses the IEEE-1014 VMEbus J1 backplane but the VME specification has been substantially modified to include analogue and fast logic (ECL) lines directly on the backplane. Furthermore, the signal line assignments on the connector differ from the VME J1 definition and a synchronous protocol is used for data transfers.

This section reviews the architecture and the functional specification of the Easybus.

4.5.2.1 Mechanics

The Easybus is used in an Eurocrate environment. The modules have the standard VME height of 233 mm but are 220 mm deep (as opposed to 160 mm for normal VME modules) to provide enough room for the electronic components. A 21-slot VME J1 backplane is mounted in the lower portion (P2) of the subrack. As the contact assignments differ from the VME spec. , the standard VME terminating networks must be removed. Resistors mounted on the Controller Card ensure that the data transfer signal lines rise to a high logic level when they are in the idle state. Pull-down resistors are connected to the ECL lines. The upper portion (P1) of the subrack is free and can be used for additional input/output connections. To facilitate cabling operations, the power supply is installed in the P2 portion behind the backplane.

4.5.2.2 Signal Lines

The following table identifies the Easybus signals by signal mnemonic and describes their characteristics. Table 4.2 gives the contact assignments on the backplane connector[3].

Signal mnemonic	Signal name and description
A01 - A16	ADDRESS BUS - 16 address lines driven by the Controller Card.
D00 - D15	DATA BUS - Three-state driven bidirectional lines used to transfer data between the Controller Card and an Easybus module.
ENA*	ENABLE - A strobe line driven by the Controller Card. During a write cycle, a low level indicates that valid address and data are available on the bus. On a read cycle, a low level indicates that the address is valid.
DCk*	DATA CLOCK - A strobe line driven by the Controller Card to trigger the loading of registers, memories...
R/W*	READ/WRITE - A signal generated by the Controller Card to indicate whether the data transfer cycle is a read or a write. A high level indicates a read operation.
RESP	RESPONSE - An analog line driven by the slave module(s) which is (are) addressed. The signal level is decoded by the Controller Card to distinguish between no, single, or multiple responses.
HCk±	HERA CLOCK - Two bipolar ECL lines that transmit the permanent 10.4 MHz clock signal to the Easybus modules. The significant edge is the rising edge of the HCk$^+$ signal.
PEN±	PIPELINE ENABLE - Two bipolar ECL lines that broadcast to the Easybus modules the pipeline gate signal driven by the Subsystem Trigger Controller. A falling edge on the PENline indicates a L1keep.
HCR1* - HCR4*	HERA CLOCK RELATED SIGNALS - Four signals that the Controller Card receives from the STC and broadcasts over the Easybus. In the crates housing the Receiver Cards,

[3]A * in the signal mnemonic means an active low signal line, i.e. a high (low) logic level is translated to a low (high) electrical level.

	the HCR2* and HCR3* lines are used to distribute the test-pattern and test-pulse signals.
SYR*	SYSTEM RESET - An open collector signal driven by the Controller Card and the power supply control unit which, when low, causes the system to be reset.
ANA±	ANALOG - Two lines for analog measurement by the ADC on the Controller Card.
+ 5 V	+ 5 VDC Power
- 5.2 V	- 5.2 VDC Power
GND	The DC voltage reference for the Easybus system.

4.5.2.3 Electrical Specifications

1. The signals A01-A16, D00-D15 conform to HCTMOS levels. The signals DCk*, ENA*, R/W* conform to HCMOS levels .
2. The RESP line is driven by open-collector gates. A 330 Ω pull-up resistor on the Controller ensures a + 5 V level when the line is not driven. The Easybus Cards that decode a valid address pull the line down through 470 Ω resistors. The resulting voltage level is measured by two fast comparators on the Controller Card in order to determine the number of selected cards.
3. The HCk± and PEN± signals are driven by a MC10H114 circuit. Pull-down resistors are installed on the Controller Card.
4. The HCRn* signals are TTL driven by a MC10H125.

4.5.2.4 Timing

The timing rules that govern the data transfers between an Easybus slave module and the Controller Card are described in this paragraph. A synchronous scheme involving two timing pulses is specified. The timing relationships are illustrated in figure 4.10

4.5.2.4.1 Write cycle

1. The Controller drives the address, data and R/W* lines to a stable state. The moment when the signals are stable is called T0.

Pin number	*Row a signals*	*Row b signals*	*Row c signals*
1	D00	(free)	D08
2	D01	(free)	D09
3	D02	(free)	D10
4	D03	(free)	D11
5	D04	(free)	D12
6	D05	(free)	D13
7	D06	(free)	D14
8	D07	(free)	D15
9	Gnd	(free)	Gnd
10	HCk$^+$	(free)	HCk$^-$
11	Gnd	(free)	Gnd
12	PEN$^+$	(free)	SyR*
13	PEN$^-$	(free)	Gnd
14	R/W*	(free)	HCR1*
15	Gnd	(free)	HCR2*
16	DCk*	(free)	Gnd
17	Gnd	(free)	HCR3*
18	Resp	(free)	HCR4*
19	Gnd	(free)	Gnd
20	Ena*	(free)	Ana$^+$
21	(free)	(free)	Ana$^-$
22	(free)	(free)	A16
23	Gnd	(free)	A15
24	A07	(free)	A14
25	A06	(free)	A13
26	A05	(free)	A12
27	A04	(free)	A11
28	A03	(free)	A10
29	A02	(free)	A09
30	A01	(free)	A08
31	- 5.2 V	- 5.2 V	- 5.2 V
32	+ 5 V	+ 5 V	+ 5 V

Table 4.2: Easybus pin assignments

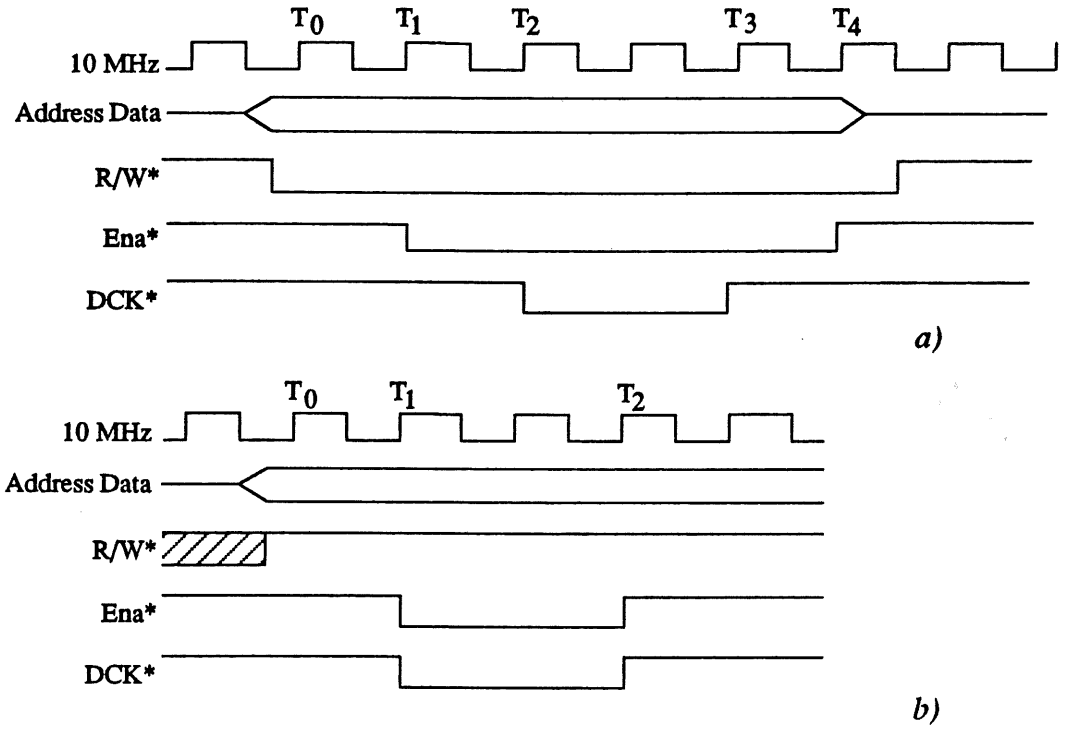


Figure 4.10: Easybus data transfer. a) Write cycle. b) Read cycle

2. The Easybus cards monitor these lines continously and respond with the RESP signal. The Controller senses the status of this line. With 0 or > 1 cards responding no data transfer is started and a timeout error occurs if the transfer was initiated from the VMEbus. With valid response the ENA* signal is driven low. This time is called T1.

3. On recept of a ENA* low signal, the addressed card enables its data transceivers in the backplane to card direction.

4. At time T2 (typically T1 + 100 ns), the DCk* signal is asserted for 200 ns. Addressed D-type registers strobe the data in at T2, and latches will be transparent between T2 and T3.

5. At a time T4 = T3 + 100 ns the cycle is terminated and the ENA* signal is removed. The Controller may change the lines and start a new cycle.

4.5.2.4.2 Read cycle

1. The Controller asserts the address and R/W* lines to a stable state. The moment when the signals are stable is again called T0.

2. The Controller senses the status of the RESP signal. If 0 or > 1 cards respond the cycle is aborted and a timeout bus error occurs if the cycle was initiated from the VMEbus. With a valid response the ENA* and DCk* signals are both driven low. This time is called T1.

3. On receipt of ENA* and DCk* low, the addressed card enables its data transceivers in the card to backplane direction.

4. At a time T2 (typically T1 + 200 ns), the Controller strobes the data in and the ENA* and DCk* are negated.

4.5.3 The STC Interface

The STC interface distributes on the Easybus the trigger-related signals broadcast by the Subsystem Trigger Controller, with in particular the HERA clock HCk and the pipeline gate signal PEn. The connection between the Controller Card and the STC is made by a 2 × 10-pole flat cable plugged into a front-panel connector and a Fanout Card output port. On the CC, the differential signals are converted either in bipolar ECL (HCk, PEn) or in TTL levels (HCRn signals). A programmable delay of maximum 126 ns with steps of 2 ns may be introduced into the HCk path. The active polarity of the HCRn signals can be selected by bridging pins in a jumper field.

4.5.4 The ADC

The Easybus has two auxiliary lines which allow the measurement of bipolar analog voltages on the Receiver Cards. These lines are connected to the ADC of the Controller Card through low-pass filters and a differential sample/hold circuit to reject the common-mode noise. The conversion is performed by a Burr-Brown ADC80AG-12 with the following specifications:

- Successive-approximation conversion.
- 25 μs maximum conversion time.
- Resolution of 12 bits.

The ADC offers two input ranges: ± 5 V or ± 10 V. The appropriate range is selected by a jumper field. Ror more information about the analog measurement. Refer to the description of the Receiver Card (see 3.6).

4.6 The Subsystem Trigger Controller

4.6.1 Introduction

The Subsystem Trigger Controller (STC) acts as the interface between the Central Trigger Controller (CTC) and the MWPC readout system [51]. It is housed in a 21-slot double height crate equipped with a VME backplane in the J1 position and with five-row Euro connectors in the bottom part. These latter are used to connect the STC modules to the CTC drivers via twisted-pair cables and to pass control lines between the STC modules via wire-wrapped connections. The communication path with the Master Crate is provided by a two board set from VMIC [52] which allows VME slave boards in the STC crate to be controlled by the readout controller. On the VMIC boards, the VME signals are just buffered so that the STC VME backplane appears as an extension of the master backplane. As the J2 backplane is missing in the STC crate all VME transfers to this crate are restricted to 16 data and 24 address bits.

The two main functions of the STC are to distribute to the front-end modules various control signals (HCk, Test pulses ...) and to synchronize the FIC 8232 and the BDCs with the trigger sequence. In normal data taking mode, the STC is controlled by the Central Trigger Controller with a handshake protocol. For test purposes on board logic is provided which allows to run the STC as a stand-alone controller. In this way the MWPC system can be debugged or tested in various modes independent of the central logic.

The STC receives from the CTC the machine-related signals (HERA clock, bunch current information ...), the trigger signals (L1keep, PEn ...) and some run control lines (e.g. prepare and stop run). To the CTC, it transmits the status of the readout system (ready or busy) and acknowledges the service requests. With the readout controller, the STC communicates through VME data transfers and interrupts.

The STC functions are provided essentially by a set of 4 modules which are described below.

4.6.2 The Fast Card

The Fast Card [53] is the central module of the STC. It contains the following functional blocks (see figure 4.11) :

- A CTC interface which receives the "fast outward" signals broadcast by the Central Controller (HCk, PEn, L1keep ...)

- A local trigger sequencer and various simulators for machine signals to be used in test mode.
- A handshake logic to signal the status of the subsystem to the CTC.
- A set of scalers which count the bunches and the beam revolutions within HERA.
- A STC interface which passes on the J2 connector various signal lines which can be connected via a wire-wrap technique to the other STC modules.

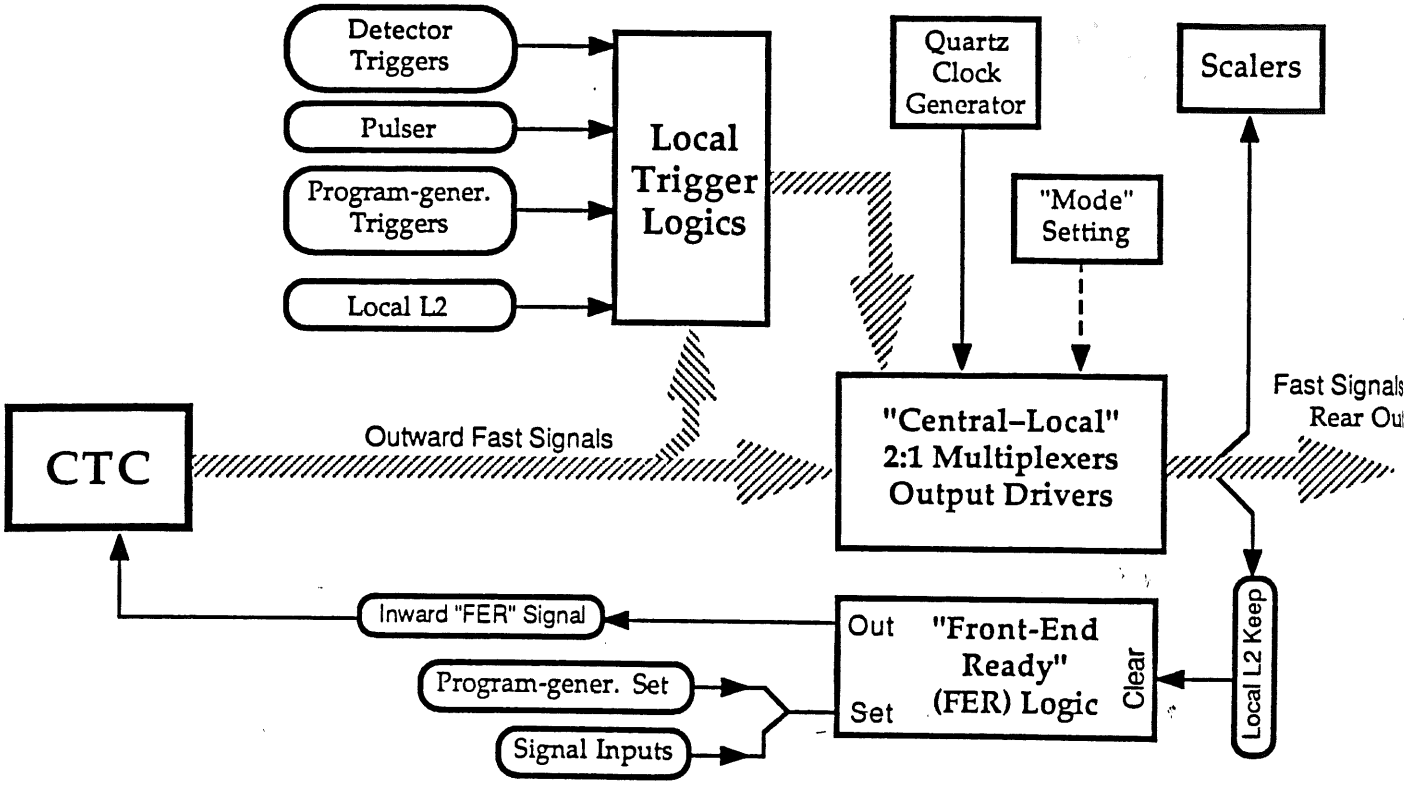


Figure 4.11: Schematic overview of the Fast Card

The multiplexing between central and local signals is controlled by the operation mode of the STC. There are five possible modes, numbered from 0 to 4, which correspond to different levels of dependence on the CTC :

mode 0 : CTC submissive. All the signals are received from the CTC. It is the normal data taking mode.

mode 1 : Data autonomous, trigger submissive. The STC receives the clock and the trigger signals from the CTC as in mode 0 but the central

logic does not care whether the subsystem is ready for data taking or not.

mode 2 : Data and L2 autonomous, L1 submissive. Similar to mode 1, but the STC does its own L2 decision.

mode 3 : Trigger autonomous, clock submissive. In this mode the actions of the STC are completely independent of the CTC. The trigger sequence is controlled by local logic, for example by a NIM-based detector trigger or a pulse generator. However, the 10.4 MHz clock is still received from the CTC.

mode 4 : STC autonomous. Similar to mode 3, but the clock signal is also taken from a local oscillator. This mode of operation is used when the CTC is not operating.

In practice, only the modes 0, 3, and exceptionally 4, are used.

4.6.3 The Slow Card

The Slow Card [54] is used to synchronize the data acquisition with the trigger signals broadcast by the CTC. The module acts as an interrupt generator with a set of 9 interrupt channels driven either by the CTC (mode 0) or locally through VME commands (mode $\neq 0$). A wire-wrapped matrix allows to connect each interrupt channel to one of the VME I4–I7 interrupt request lines through a priority encoder. During data taking, an interrupt cycle is initiated by setting the input register controlling an interrupt channel. Six STC interrupt sources are presently defined and recognised by the readout controller (see table 4.3).

Interrupt	*Channel*	*Level*
Prepare run	3	4
Terminate run	2	4
Status	4	4
L2keep	8	4
L3keep	1	5
L3reject	0	5

Table 4.3: Interrupts on the Slow Card

In response to the assertion of an interrupt, the readout controller executes a VME interrupt acknowledge bus cycle to read the vector number identifying the interrupt source. Depending on the source the readout controller performs the required actions, for example system initialisation, L2keep handling. Once the interrupt has been served, the controller resets the corresponding interrupt register on the Slow Card. This signals to the CTC that the request was acknowledged. Note that the L2keep interrupt is special and is acknowledged by setting the FER signal on the Fast Card. This procedure is detailed in 4.8.3.3.

In addition to the interrupt circuits, the Slow Card also contains two 32-bit counters for counting the L1keep and L2keep triggers.

4.6.4 The Fanout Cards

The Fanout Cards [55], [56] distribute the internal STC signals to the MWPC electronics in NIM and differential forms. Each card has 5 cable ports through which 6 signals may be broadcast outwards and 2 received by the STC. Two of the outward lines are firmly allocated to the HClk and PEn signals. The others, called "slow 1-4", can be used for any purpose in the system. For instance, the slow 2 and slow 3 signals are used to control the test-pattern and test-pulse circuits on the Receiver Cards. Elements for delaying, gating and simulating these signals are provided on the module.

Four Fanout Cards are used to operate the front-end electronics : one for each of the MWPC detector group and one for the TOF counters. In addition, two Fanout Cards are used for the trigger electronics and one to control the DMAC installed on the branch drivers. This partition is summarized in table 4.4.

4.6.5 The Triggerbit Card

The triggerbit Card [57] receives, under control of the Central Trigger Controller, the information indicating which trigger condition has caused a L1keep. The data are read via VME and serves as a check for the correct operation of the STC. These data are also used by the MWPC on-line monitoring system for the event analysis.

Card	*Receiver*	*Function*
1	FPC receiver cards	Distribution of the HCk, PEn, test-pulses and test-pattern signals.
2	CPC receiver cards	idem.
3	BPC receiver cards	idem.
4	Forward ray trigger	Distribution of the HCk and PEn signals.
5	Z-vertex trigger	idem.
6	BDCs	Control of the BDC DMAC request lines.
7	TOF receiver cards	Distribution of the HCk and PEn signals.

Table 4.4: Fanout Card partition

4.7 Commercial Components

4.7.1 CPU Boards

The MWPC readout controller is a FIC 8232 board from CES [58]. It is a 32-bit VMEbus single board computer based on the MC68030 microprocessor clocked at 24 MHz. A block diagram of this module is shown in figure 4.12.

The MC68030 is a second generation full 32-bit enhanced member of the M68000 family from Motorola. It combines a central processing unit core (CPU), a memory management unit (MMU) and 256-byte instruction, MMU and data caches in a single VLSI device. To enhance the performance when running floating point calculations, the MC68030 can accommodate up to 8 coprocessor types in one system. On the FIC 8232 one socket is provided for a MC68882 floating point unit.

The microprocessor bus is directly connected to a local static RAM memory and an EPROM which both can be accessed by the CPU without wait state. These memories are used to store the firmware monitor, frequently used tasks and programs requiring maximum execution speed. To enhance the block transfer throughput of the system, the CPU bus also supports a 32-bit DMA controller. This latter contains specialized hardware that allows to perform data transfers between on-board, VME and VSB memory arrays at a higher rate than the CPU. A SCSI interface and a general purpose connector are attached to this controller through an 8-bit peripheral bus. This allows to couple external input/output devices, such as tape or disk controllers, to the system bus. Furthermore, data

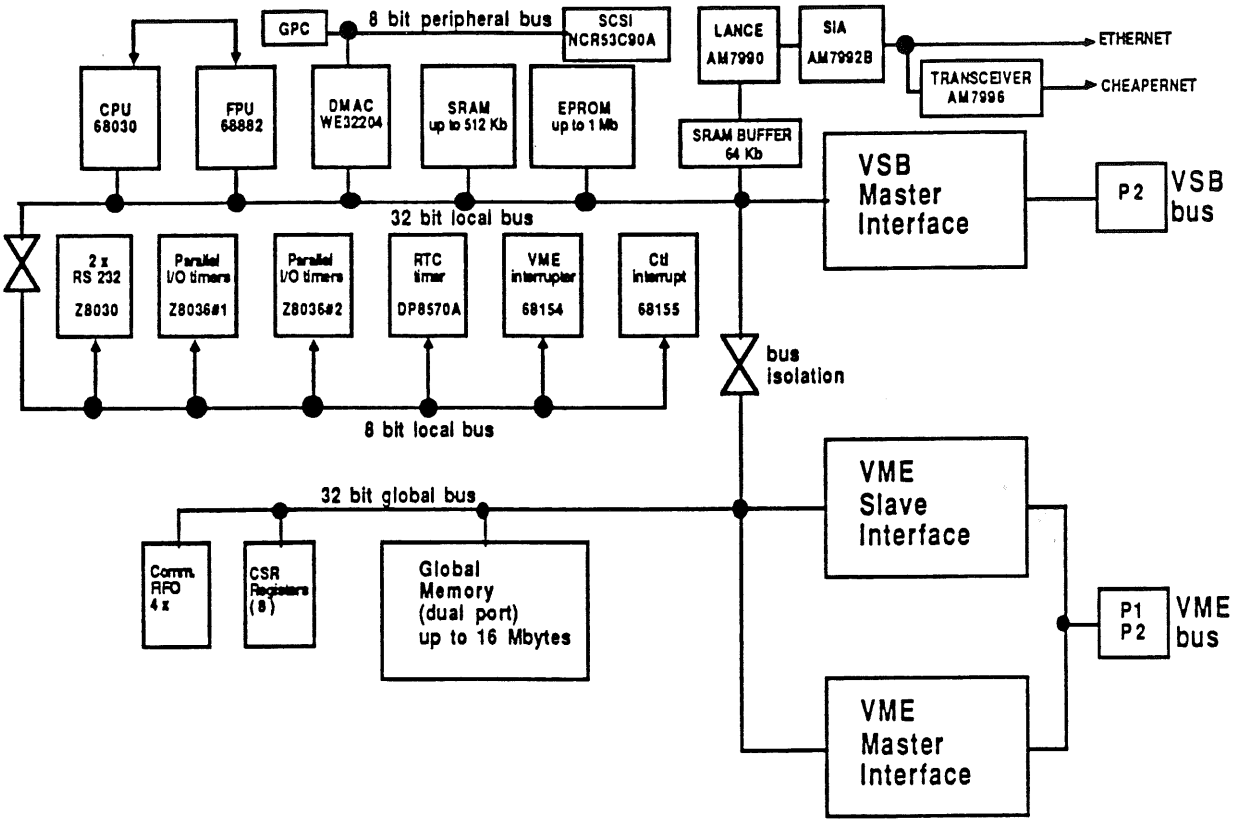


Figure 4.12: Block diagram of the FIC 8232

exchange between the 68030 and an Ethernet network is supported by a specialized local area network controller (LANCE) with an on-chip DMA channel. This controller is isolated from the CPU/DMAC bus by a 64-kbyte dedicated buffer to increase the system performance. An 8-bit local bus is derived from the 32-bit CPU bus. It supports the serial link controllers, primary used for terminal and host connections, the interrupt controllers and various event counters and timers.

Access to and from the VMEbus is provided by a 32-bit global bus which can be driven either by the 32-bit local bus or by external processors using the VME slave interface. This bus supports a dual-ported RAM, used as the main system memory, control and status registers, and four communication FIFOs. The latter may be used as mail-box memories in a multi-processing environment.

The processor board running the on-line monitoring program is a FIC 8230 based on the MC68020 microprocessor. This module is the ancestor of the FIC 8232. It has the same architecture except that no SCSI and LAN interfaces are implemented.

4.7.2 Memory Boards

1. The multi-event buffer is provided by a DPM 8242 board from CES [59], a dual ported static RAM module interfaced to VME and VSB. It contains 512 kbytes of battery backed-up SRAM with an access time of 70 ns. The VME/VSB interface logic has been optimized to provide a large bandwidth for memory access. Particularly, the DPM supports the broadcast handshaking mode which allows to write a data word into several modules in one transfer cycle.

2. A SYS68K/RR-2 memory board from Force Computers [60] is used to store the program object code and the data-bases necessary for system initialisation. The board contains two independent memory areas which can be equipped with static RAM, EPROM or EEPROM. A battery back-up with a voltage sensor is installed to allow data retention for the SRAM devices. The EEPROMs allow RAM-like access and software controlled write protection. The module installed in the Master Crate is equipped with 1 Mbyte of SRAM and 512 kbytes of EEPROM.

3. The monitoring crate is equipped with a SYS68K/DRAM-8 [61] on which 8 Mbytes of dynamic RAM are installed. This memory is used to extend the FIC 8230 global memory.

4.7.3 Crate and Computer Interconnects

1. A vertical bus system VIC8250 from CES [62] is used to interconnect the Master Crate with the monitoring crate. This interface system offers a transparent connection between up to 15 VME crates by means of a multiplexed cable bus ("VMIVbus"). All VME cycles are supported with a transfer rate up to 8 Mbytes/s. The VIC8250 board in the Master Crate is equipped with a triple port buffer memory of 512 kbytes mapped on the VME, VSB and VMV busses. This memory can be used as a shared data area for multiprocessing operating systems or as data buffer between VME crates. Part of the buffer memory is assigned to 8 mail-box flags that can generate interrupts over the VME, VSB or VMV. This mail-box is used for message exchange between the readout controller and the monitoring processors.

2. The connection between the Master Crate and the STC is performed by a VMIVME Repeater Link from VMIC [52]. This link consists of a software transparent two-board set that allows to extend a VMEbus chassis to additional slots in another crate. The extended slots, however, are only operational for VMEbus slave modules. The Repeater Link supports 32-bit data transfers and all seven interrupt levels.

3. The Macintosh computers are connected to the VMEbus via a MICRON/MacVee two board set [35]. This link provides direct memory access from a Macintosh NuBus slot with up to 8 VME crates. The system supports all 68020 based data transfer operation types in a 24-bit addressing range. The required VMEbus operations are automatically performed so that the interface is transparent to the users.

4.8 Synchronization Mechanisms

4.8.1 Introduction

The correct acquisition of the event data, i.e. the collection of data belonging to the same bunch crossing (BC), requires a precise synchronization of the complete readout system. For instance, the discriminated detector data must be latched in registers labelled with an unique time tag in order to keep the time correlation between event signals and the bunch structure of the HERA machine. This correspondence between data and bunch crossing time has to be preserved throughout the whole readout chain until all detector data are structured, according to detector group and BC number, in event records stored in the MEB. Subsequently, these event records are labelled with an event number, allowing the central event coordinator to assemble the data blocks from the different sub-detector memories into a full event record that contains all information for a single event.

The synchronization tasks, as well as the coordination of the readout with the triggering levels, are completely managed by the Central Trigger Controller via the local STC system. This section reviews the implementation of this mechanism. The control of the front-end pipelines is discussed first. Next, the readout sequence is detailed together with an introduction to the data acquisition software.

4.8.2 Front-end Synchronization and Pipeline Control

The alignment of the data by bunch crossing in the front-end pipelines (FEP) is controlled by 2 signals (see figure 4.13) :

- The 10.4 MHz HCk square wave that times the synchronizer circuit and controls the shift of the data in the pipeline.
- The PEn signal which controls the transition between the acquisition and readout modes (see 3.6.3).

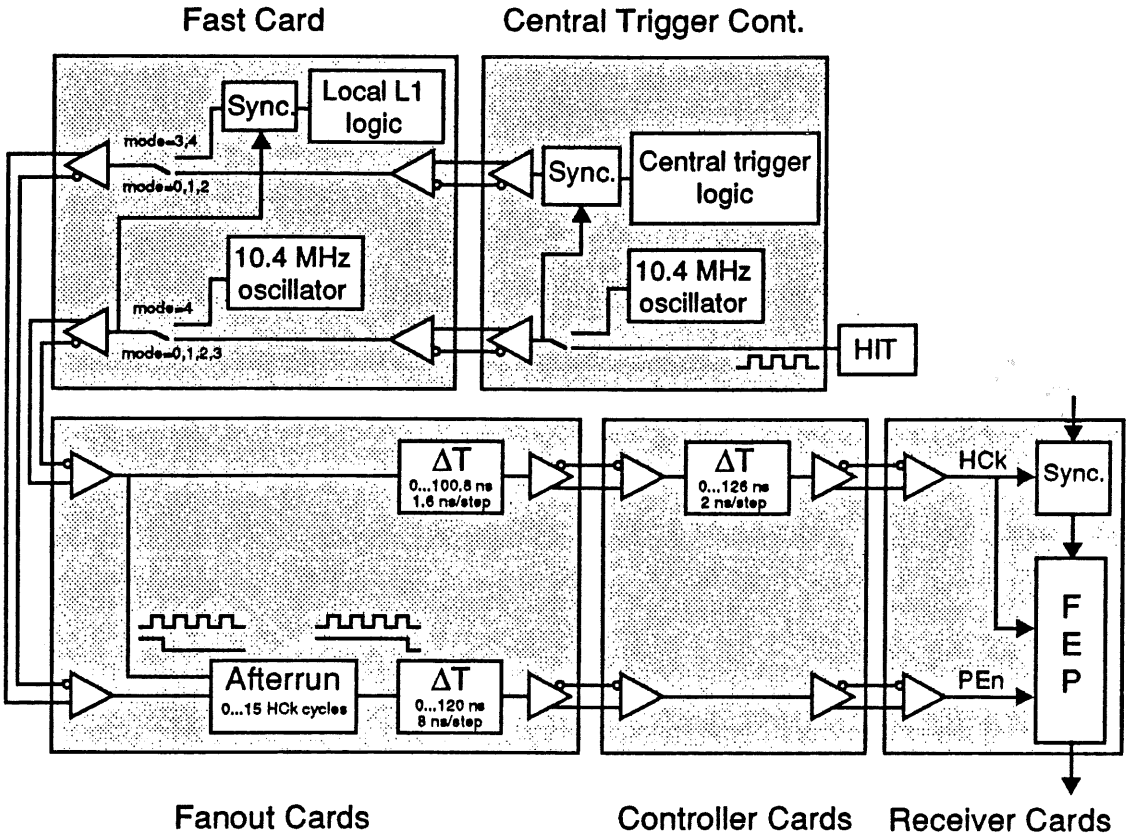


Figure 4.13: Front-end pipeline control layout

In normal data taking mode (STC mode 0), these signals are distributed by the CTC to the Fast Card. The HCk clock is generated by the HERA Integrated Timing (HIT) system located in the accelerator control area (West hall) and transmitted in a star-like fashion to the experimental halls over glass-fibres. Its phase is fixed to the bunch crossing with an accuracy of about 1 ns. When there is no beam, an artificial clock signal can be generated either in the CTC (mode $\neq 4$) or on the Fast card (mode 4) by a quartz oscillator. The PEn signal is derived from the L1keep signal. It is generated by the CTC in the L1 submissive modes (0, 1, 2) or by the trigger logic installed on the Fast Card in modes 3 and 4. The PEn signal is high when the L1 trigger electronic is active and goes to false when an event candidate is detected. This transition is synchronized with the 22nd HCk falling transition following the triggering event bunch crossing.

The HCk and PEn signals are distributed to the Fanout Cards where they can be delayed by means of software programmable delay units. In particular, each Fanout Card has a "PEn-Afterrun" counting register initialised at run start time with a predetermined value indicating a number of clock periods. Each time a L1keep occurs the PEn true-to-false transition is delayed by this number of clock

periods, allowing the data to be shifted to the end of the pipeline where they can be read. In order to study the event "time history" around the triggering BC, one wants not only the data of the triggering BC but also the information of the N_{before} time slices. To get the pipeline data correctly positionned for the readout, the Pen-Afterrun register must be loaded with :

$$N_{afterrun} = 8 - N_{before} \tag{4.1}$$

The delayed signals are distributed to the 17 Controller Cards by twisted-pair cables which have all the same length in order to maintain the timing adjustments in the STC Crate. An additional programmable element on the CC allows to adjust the relative delay of the HCk signal between front-end crates driven by the same Fanout Card.

The delay elements along the HCk signal path are set so that the signals from a given bunch crossing are synchronized in a single catching window of the Sync.GA circuit (cf. 3.6.3). In this way, every pulse fed into the trigger logic is uniquely associated to the correct bunch crossing number and data from consecutive crossings are stored in consecutive registers in the pipeline. Once the HCk phase is correctly adjusted, the timing of the PEn true-to-false transition has to be fixed. Indeed, for proper operation of the shift register the signal at the M0 input of the pipeline may only change state in a restricted phase window of HCk, as shown in figure 4.14.

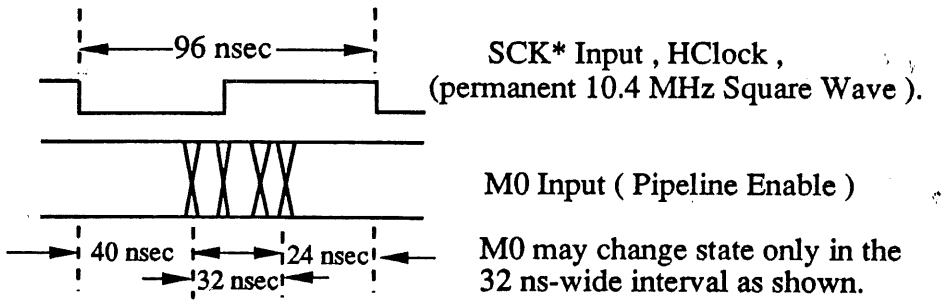


Figure 4.14: Timing of M0 transitions relative to HCk

Figure 4.15 shows typical distributions of hits in the pipelines when all these parameters are properly adjusted. The readout conditions were : $Nbc = 10$, $N_{before} = 6$. A peak in bin 6, which corresponds to the 22nd register in the pipelines, is clearly visible in the distributions. Data in other time slices come from non-triggering bunch crossings and from noisy channels. These plots demonstrate the ability of the MWPC detectors to provide the bunch crossing time t_0.

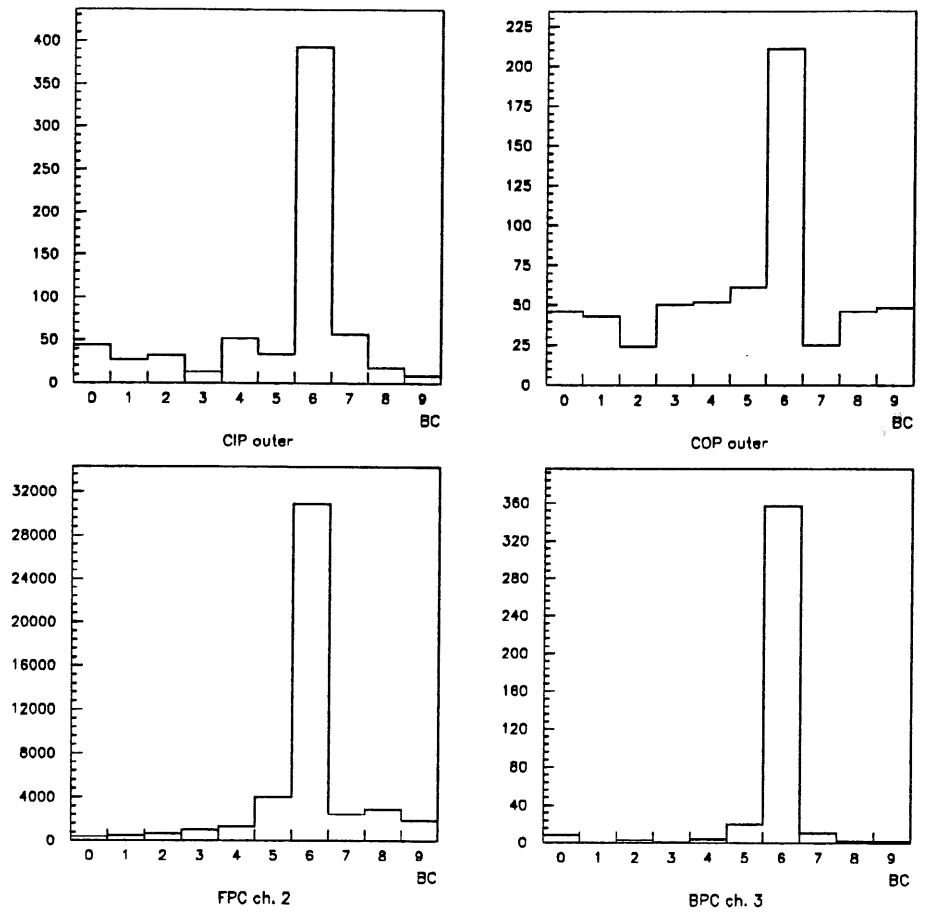


Figure 4.15: Hit distribution in the front-end pipelines

4.8.3 Readout Synchronization

The structure of the readout hardware, as defined in the previous sections, requires intensive processor intervention during data acquisition. Indeed, each time a front-end transfer takes place the readout controller has to handle the interrupts from the STC and the BDCs in parallel with the formatting of the raw event data into the multi-event buffer. In addition to this, the readout controller has to interface with the supervising Macintosh and the monitoring system and, last but not least, displays status information on its control terminal.

All these tasks have to be processed with different priority levels in order to maintain a fast real time response to the DAQ related activity. For instance, the occurrence of a STC or a BDC interrupt requires immediate attention to avoid an increase of the dead time beyond the limiting value of 0.8 ms. These requirements have led to the development of a software protocol optimised for speed and efficiency in the MWPC data acquisition environment. An introduction to this software is given below, followed by a description of the interrupt structure.

Next, the readout and monitoring tasks are detailed.

4.8.3.1 MWPC DAQ Software

The MWPC DAQ software is written on top of a dedicated multi-tasking system especially adapted for data acquisition [63]. The system is interrupt driven and schedules tasks in function of their software priority. Its main characteristics are summarised below :

- The scheduler operates every 100 ms. This low rate minimises the system overhead and insures nevertheless a fast user response. Fast response to the DAQ related interrupts is ensured by the fact that these interrupts call the scheduler when the DAQ task is not the active one.
- The scheduler has a fast and simple algorithm. Each task preserves its running priority and is scheduled according to this priority. The highest priority task that is not suspended takes all of the run time. Tasks having the same priority are scheduled in a round-robin fashion.
- The tasks run in user mode whereas the scheduler executes at the supervisor privilege level. A-trap instructions are used to switch from the user to the supervisor privilege level.

The communication protocol with external processors relies on the exchange of directives, consisting of command identifier and parameters, through dual-ported mail-box memories. For instance, message passing with the CDAQ and the monitoring system is done through dedicated memory blocks in the MEB and the Master Crate VIC buffer respectivelly. Data exchange with the supervising Macintosh is implemented by using the FIC communication FIFO buffers. Dedicated software libraries [63], [64] provide routines catering for all essential functions such as system initialisation, status information, error handling....

All the on-line code is written in Assembler. Development instruments are installed on the Macintosh computers so that no sophisticated programming package is required to run on the FIC board. The VMEUA1MON [36] facility on the FIC is used for debugging and to enable the basic CPU functions (start, memory dump...).

4.8.3.2 Interrupt Structure

Figure 4.16 shows a schematic diagram of the hardware interrupt structure used to drive the DAQ software. The various interrupt generators are listed below:

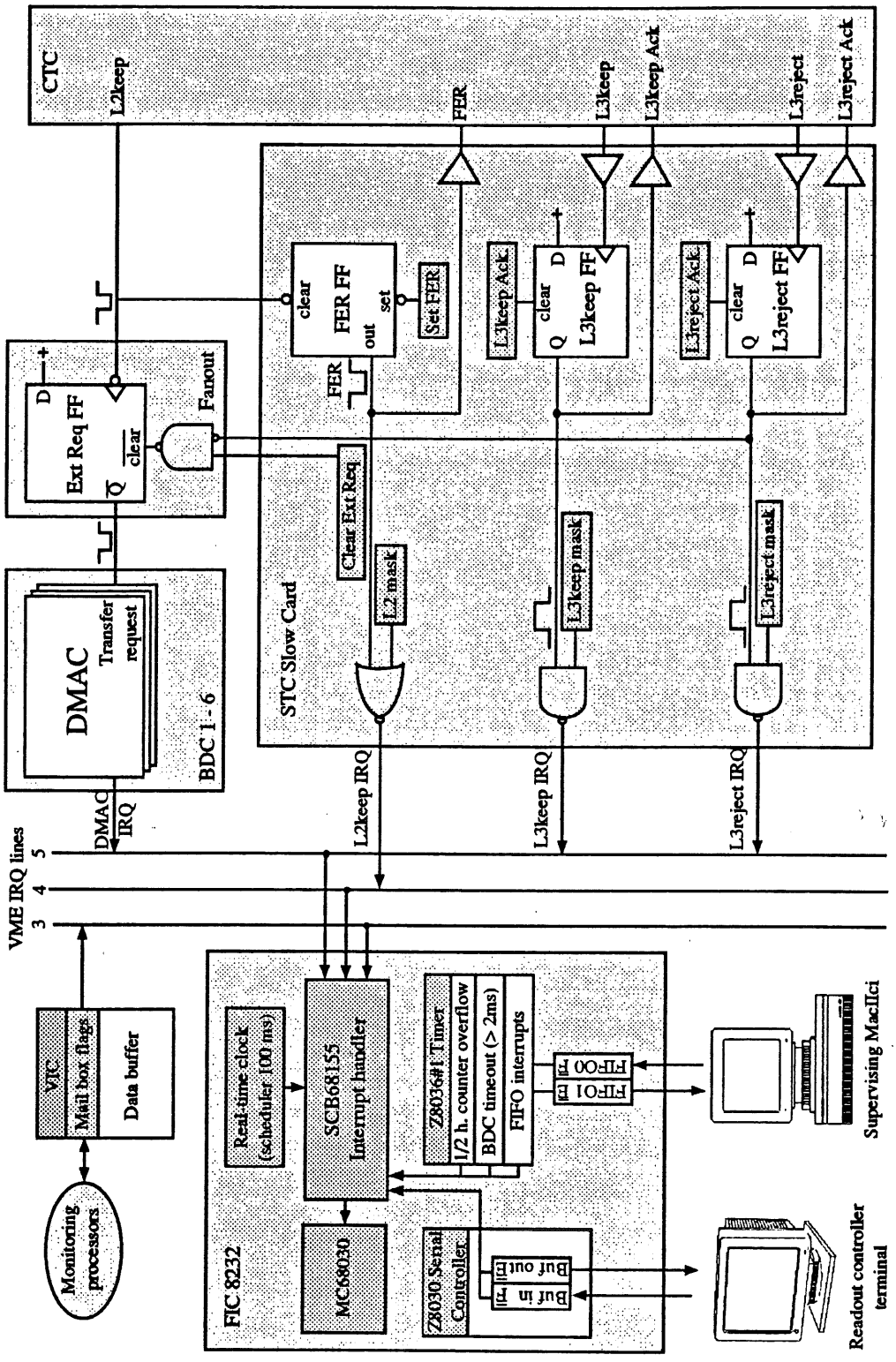


Figure 4.16: Interrupt structure in the MWPC readout system

- The real-time clock device (DP8570A) calls the scheduler every 100 ms.
- The Z8030 serial controller requests interrupt service when its transmit buffer becomes empty or when a character loaded in the receive buffer is ready to be read. This communication mode allows to exchange data with the terminal, a very slow device, without introducing large software overheads.
- The Z8036♯1 timer has many functions. It interrupts the CPU when the communication FIFO buffers contain data from the MacII (FIFO 0 full) or when data transmitted to the MAC have been read (FIFO 1 empty). It also gives a time-out interrupt when a front-end DMA transfer does not complete in 2 ms. Its internal time counter, used for monitoring purposes, interrupts when it overflows.
- The Master Crate VIC8250 module generates an interrupt request when its dedicated mail-box flag is set in the on-board buffer by a monitoring processor requesting data.
- Each DMA controller on the branch drivers interrupts the CPU either on completion of the front-end transfer or when an error condition has occurred.
- The STC Slow Card generates interrupts on the occurrence of the L2keep and L3keep/L3reject and to signal a Start/Stop of run.

The handling of the DAQ related interrupts (DMAC, STC) is detailed in next section.

The different interrupt sources described above are processed by the FIC interrupt handler circuit (SCB68155) into level categories which ensure proper priority at the level of the CPU. The real-time clock has the highest priority : level 6. The serial controller and timer interrupts are connected to level 3 and are daisy-chained. The VMEbus interrupt requests have the same level as the sources : DMAC and L3keep/reject on level 5, L2keep on level 4, VIC mail-box on level 3. The daisy-chain priority structure of the VMEbus ensures that the different level 5 interrupters are priorized according to their physical position in the backplane : BDC 1 to 6 followed by the STC Slow Card.

4.8.3.3 Readout Cycle

The actions associated with the data acquisition are described in this section. The timing relationships are illustrated in figure 4.17. Timings are given for the readout of 10 bunches centered around the triggering event bunch crossing. The data acquisition operates in three consecutive phases :

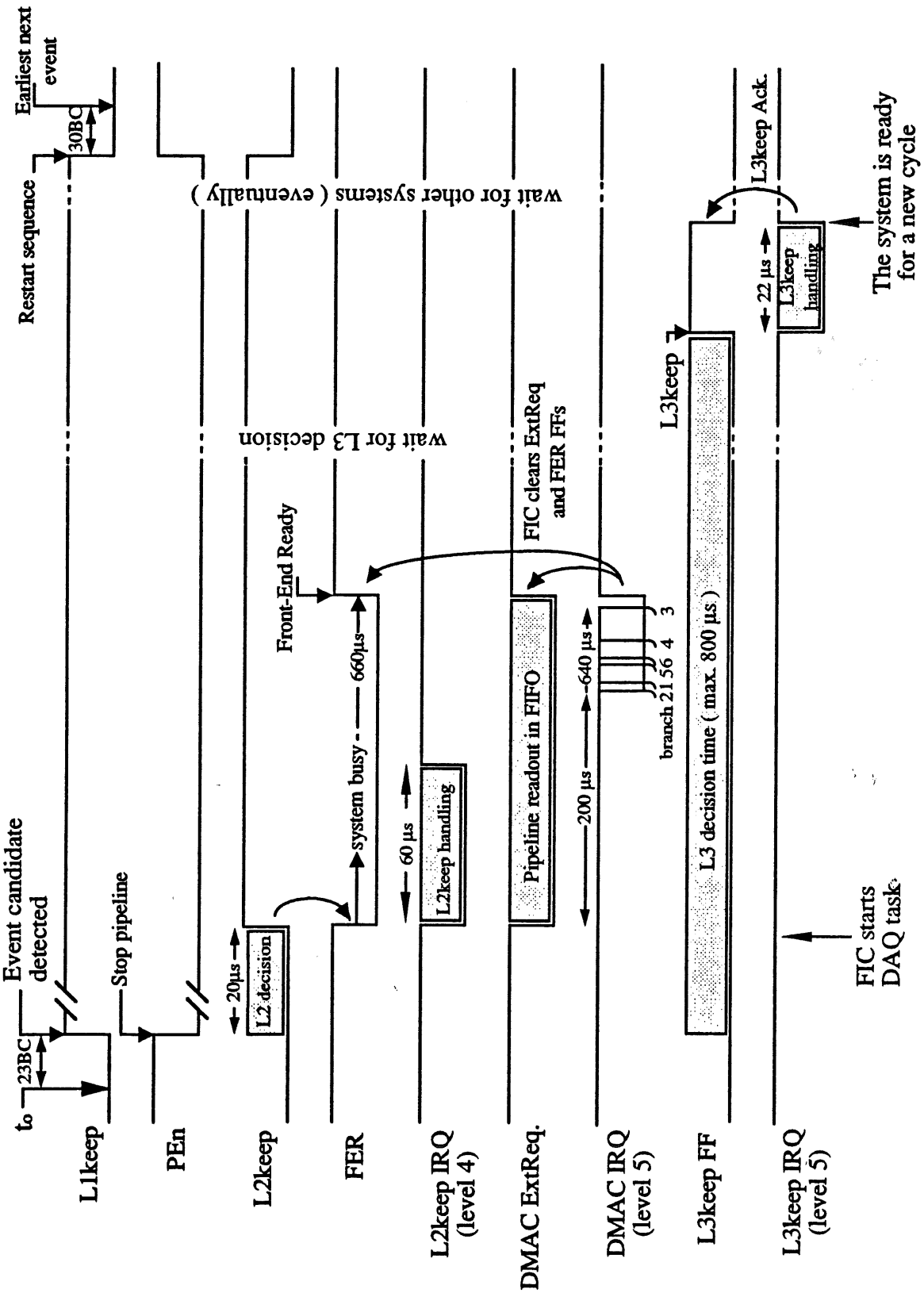


Figure 4.17: Time diagram of a readout cycle

1. The run start phase

   In this phase, all the hardware components are initialised according to the description contained in the data-base loaded in the SYS68K/RR-2 memory. Software tables are built with quantities frequently used during the run. A run start record with the parameters of the run (readout configuration, threshold values...) is sent to the CDAQ.

2. The run phase

   After the run start, the DAQ task becomes idle until an event related interrupt activates it. The front-end ready (FER) flip-flop is set high, indicating that the system is ready to accept a new event. If an event candidate is kept by the L2 logic, then the L2keep signal goes to true. This clears the FER flip-flop and causes the BDC DMACs to automatically start transferring the front-end data over the vertical branches. Consequently, a VME level 4 interrupt is generated which activates immediately the DAQ task on the FIC. About 60 μs are then necessary to read the STC scalers, to update various runtime parameters and to read timers for local system monitoring. When this is done, the FIC masks the L2 interrupt in the STC in order to release the VME IRQ4 line. About 160 μs later, the first BDC (branch 2, see 4.9) has finished the front-end transfer and interrupts the processor on level 5. The software keeps track of the interrupt and re-initialises the DMAC for the next event transfer. From this moment the processor starts or continues the readout of the FIFO and the treatment of the data. This process is regularly interrupted by the next DMAC interrupt until 640 μs after L2keep. The last BDC (branch 3) giving an interrupt controls in addition whether all BDC FIFOs can hold a complete new event. If this is possible, the FER flip-flop is set to indicate to the CTC that the front-end system is ready to accept a new event. Otherwise the oldest event in the FIFO buffers has to be completely treated before FER is given.

   The L3 decision signal causes also an interrupt on level 5. A L3keep interrupt is only used as a flag to indicate that the event has to be sent to the CDAQ for further filtering. On the other hand, a L3reject signal stops automatically all running BDC transfers. The interrupt handler then records the state of each DMAC to determine the amount of data words already transferred in each FIFO. This information will be used asynchronously to flush the L3reject data when they are available at the FIFO output. After re-initialisation of each BDC, the FER signal is given if a complete new event can be stored in the FIFOs. When the L3 interrupt handling is finished, the corresponding L3 flip-flop is cleared. At that time, the CTC considers that the MWPC system is ready to start a new readout cycle. When all the other subsystems have set the FER signal and acknowledged the L3 signal, the CTC initiates a restart sequence. The trigger signals are reset and the pipelines re-enabled.

The L1 logic is re-activated a few μs later when the pipelines are completely filled with new data.

3. The run end phase

   In this phase a run end record is built and all buffers and tables become obsolete.

4.8.3.4 Monitoring Interface

The monitoring interface consists of two parts. One part is running on the MWPC DAQ FIC as a separate task and the other one is a set of library routines. The whole monitoring interface relies on the VIC8250 module. The internal memory of the VIC in the Master Crate is used as buffer for the events to be monitored and the mailbox of this module synchronizes the communication between external users of the information and the controller readout. The library routines available for the user take care of the communication. Any monitoring command interrupts the DAQ processor on level 3. The interrupt handler activates the monitoring task on the FIC. Whenever there is time in between the handling of event data, this task will execute the wanted function. The events that are copied in the monitoring buffer have the same BOS-structure as in the multi-event buffer. There are however additional BOS-banks which contain the raw data and some status information.

4.9 System Performance

4.9.1 Introduction

The two most important measures of the performance of a data acquisition system are the data throughput rate and the dead time. The data throughput rate is defined as the maximum average rate at which data can be transferred and processed by the system. It is dictated by the strong coupling existing between data transfer technology, processor board architecture and algorithm design. Dead time arises when no more data can be accepted by the system. During such period, all front-end input circuits are gated and incoming signals are lost.

The front-end electronics readout is the primary source of dead time in the H1 data acquisition system.It is often referred to as the first-order dead time. Its size is governed by the L1keep rate, the decision time and the rejection factor of the L2 and L3 trigger levels, and of course by the front-end transfer time. The actual value for the first-order dead time fraction is between 10% and 20% at a L1keep rate of $\sim$ 50 Hz (no L2 and L3 rejection). Second-order dead time results essentially

from fluctuation in the event input rate and/or data size. Intermediate buffers normally de-randomise the input arrival sequence but saturation may occur when triggers come in rapid succession. The whole system may then have considerable dead time, even if the average input rate is below the maximum rate that the system can handle. In a complex system like the MWPC DAQ, buffer saturation can arise because of the complex interaction of many different system parameters including: trigger rates, channel bandwidth, processing times, buffer and event sizes.

Understanding how changes in these parameters affect dead time is a major issue for optimising the data taking efficiency. Therefore we present below a detailed analysis of the system parameters. The characteristic timings of the front-end transfer are first reviewed, followed by the event building time. Next, the buffering in the system is discussed together with considerations about the dead time.

4.9.2 Front-end Freeing Time

4.9.2.1 DMA transfer Time

The time required to move the pipelined data into the BDC FIFO buffers is determined by the block transfer rate on the vertical bus and the amount of data to transfer.

The MC68450 DMA controller can perform data transfers using various types of protocol. On the BDC, it operates in the sequential array chaining mode with an implicitly addressed device protocol (see 4.4). During this type of DMA cycle, the DMAC drives the address bus and the control signals on the vertical bus, and synchronizes the FIFO to the pipeline so that the data can be transferred directly between them. Figure 4.18 shows the functional timing for a single read cycle. The signal protocol is as follows :

S0 The DMAC drives the address lines with values from its internal address register.

S1 No signals change and the address information propagates.

S2 The address is latched in external storage devices. The address (AS^*) and data (DS^*) strobe signals are asserted to indicate that the address is valid and that the pipeline circuit should present data on the bus. The Controller Card which is addressed starts a read cycle on the Easybus (see 4.5.2).

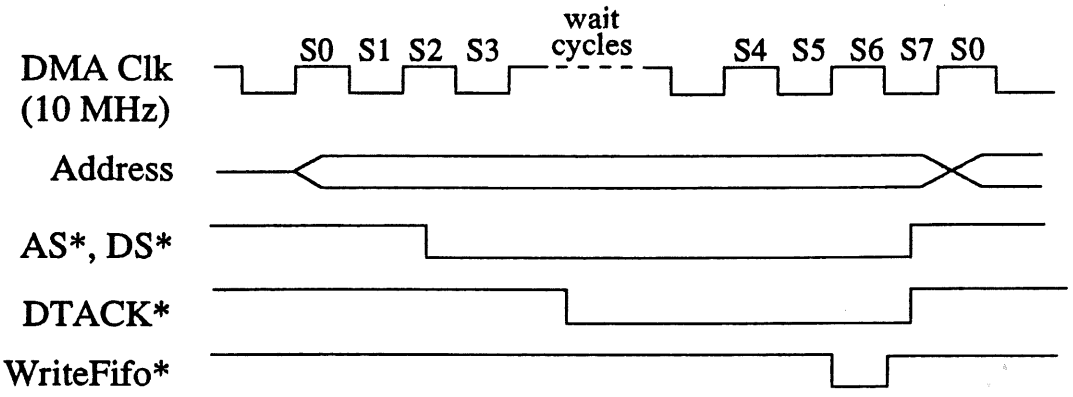


Figure 4.18: Single address DMAC read cycle timing diagram

S3 The address pins on the DMAC are three stated and the handshake signal *DTACK** is sampled to determine when the cycle should be terminated. The DMAC inserts wait cycles until *DTACK** is negated by the Controller Card to indicate that data are valid. Five wait cycles are required for the completion of a read cycle on the Easybus. This includes the signal propagation delay along the interconnecting cables.

S4, S5 No signals change during S4 and S5. The DMAC is internally synchronizing the *DTACK** signal.

S6 The data are latched in the FIFO.

S7 The strobe signals are negated to indicate that the cycle has terminated. The Controller Card responds by negating *DTACK** .

S7 + 1 This may be S0 of the next bus cycle if the DMAC is ready to execute another data transfer.

In conclusion a time of 0.9 μs is required to transfer a 32-bit data word giving a maximum block transfer rate on the vertical bus of 4.4 Mbytes/s. However, the block transfer initiation and termination operations introduce various overhead times which must be known to predict the actual front-end freeing time. Three types of overheads have to be considered (see figure 4.19):

- The front-end overhead is the delay that occurs between the time when the DMAC receives the transfer request and the time it starts a bus cycle by placing the address information on the bus. This delay is 12 clock cycles (1.2 μs) for the MC68450.

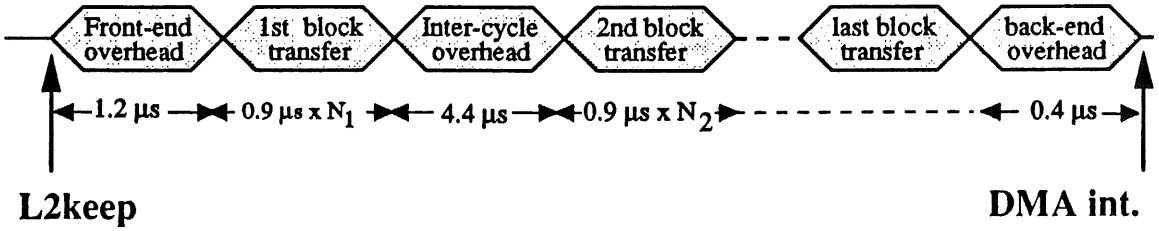


Figure 4.19: DMA operation timing

- The inter-cycle overhead is the delay that occurs between successive DMA block transfers while the DMAC maintains ownership on the bus. During that period, the DMAC reads the block descriptors in the SRAM and performs internal synchronization. Each block transfer initiation takes 44 clock cycles, that is 4.4 μs. Note that no inter-cycle overhead has to be taken into account for the first block because it is included in the channel start-up phase at the end of the previous event data transfer.

- The back-end overhead is the delay between the time when the DMAC has completed all pending operand transfers and the time it asserts an interrupt request. This delay is equal to 0.4 μs.

The front-end freeing time, that is the time between the L2keep signal and the DMAC interrupt, can now be calculated for each branch :

$$T_{L2-DMAint}\,(\mu s) = Nbc \sum_{i=0}^{Un}(0.9N_i + 4.4) - 2.8 \qquad (4.2)$$

where Nbc is the number of time slices to read ($Nbc \in [1, 30]$), Un the number of units in the branch, and N_i the number of Receiver Card pairs in unit i (refer to table 4.1). Figure 4.20 illustrates equation 4.2 for each branch in the readout.

4.9.2.2 L3keep Cycle Acknowledgment

As soon as all DMA interrupts are acknowledged, the readout controller checks if the FIFO buffers can hold a complete new event. If so it signals "front-end ready" to the CTC by resetting the FER flip-flop on the Fast Card, even if the L3 decision is not yet made (see 4.8.3.3). The time at which this instruction is executed is determined by the transfer time on the more bulky branch (CPC branch) and the interrupt handling overhead. Figure 4.21 shows this FER time T_{FER}, as a function of Nbc. A minimum delay of 430 μs is required to handle the L2keep and DMAC interrupts. If $Nbc \geq 8$ then $T_{FER} \simeq (T_{L2 \rightarrow DMAint})_{CPC} + 20\ \mu s$.

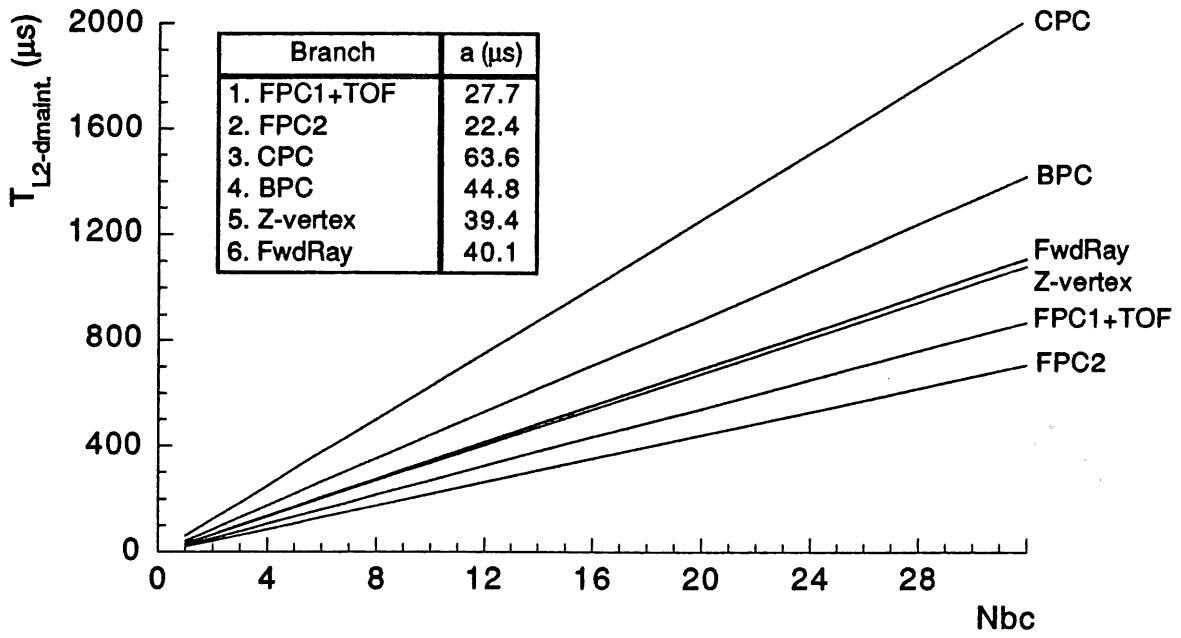


Figure 4.20: Front-end freeing time $T_{L2\_DMAint}\ (\mu s) = aNbc - 2.8$

Figure 4.21 shows also the L3 acknowledge time in the case of a forced L3keep signal at 800 μs. The L3keep flip-flop is normally reset 22 μs later, except when the DMA interrupt of the CPC branch is around 800 μs. In that case, the L3 acknowledgment is delayed by a few tens of microseconds. Nbc should not exceed 11 in order to keep the front-end readout cycle time below 800 μs.

4.9.2.3 L3reject Cycle Acknowledgment

In case a L3reject is sensed, the readout controller has to read the state of each DMA controller and mark the data to be rejected, in addition to the normal re-initialisation operations. Figure 4.22 shows the FER and the L3reject acknowledge delays as a function of the L2keep - L3reject time difference. The L3reject - L3Ack. time difference is also plotted.

Again a minimum time of 460 μs is necessary to execute the interrupt handling routines, even in the case of a very early reject signal ($<$ 250 μs). This limits the reduction of the first-order dead time that can be obtained with a L3 rejection to 40%. In the time window [250 μs, 600 μs], the acknowledge delay is around 220 μs. Late L3 reject signals ($>$ 600 μs) cause the system to generate additional dead time exceeding 800 μs (up to 950 μs).

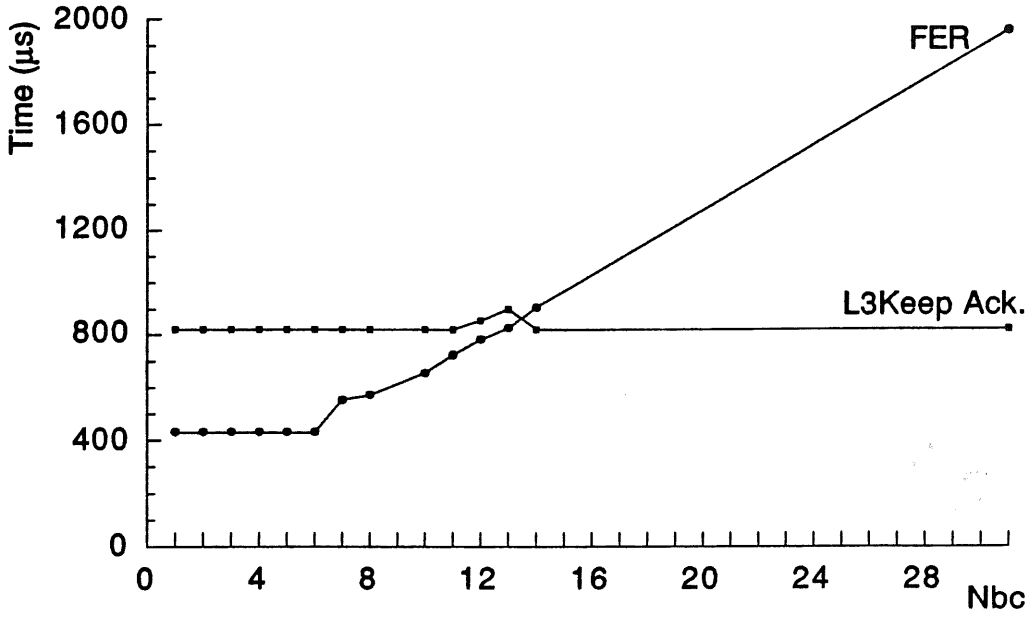


Figure 4.21: L3keep cycle acknowledgment

4.9.3 Event Building Time

When data for a triggered event are ready in the FIFO buffers, the FIC8232 processor starts the event building task. Each data block in the FIFO is then copied over VMEbus into the FIC for direct decoding and formatting. No internal buffering of the data is done in the FIC. The formatted data are assembled into a contiguous data block ("bank") into the MEB. This process is repeated for all the data blocks assigned to the same event in the FIFO buffers, in total Nbc times each active detector partition. In order to estimate the overall time required to handle a complete event, let us consider each readout partition:

1. CPC, FPC, BPC readout branches

   The bit patterns resulting from the MWPC discrimination are zero-suppressed, i.e. only the channel identifiers for which the bit is "non zero" are recorded. To speed up this zero suppression, the position of every bit in the raw data block is the offset into a lookup table which returns the channel identifier of every non zero bit. The time spent for this conversion is given by the following formula :

$$(T_{\text{FIFO}\rightarrow\text{MEB}})_{\text{MWPC}} = \sum_{\text{part=FPC,CPC,BPC}} (T_{\text{FIFO}\rightarrow\text{MEB}})_{part} = \sum_{part} \sum_{n=1}^{Nbc} (T_n) \quad (4.3)$$

   with

$$T_n = T_{\text{FIFO}\rightarrow\text{FIC}} + T_{\text{FIC}\rightarrow\text{MEB}} \quad (4.4)$$

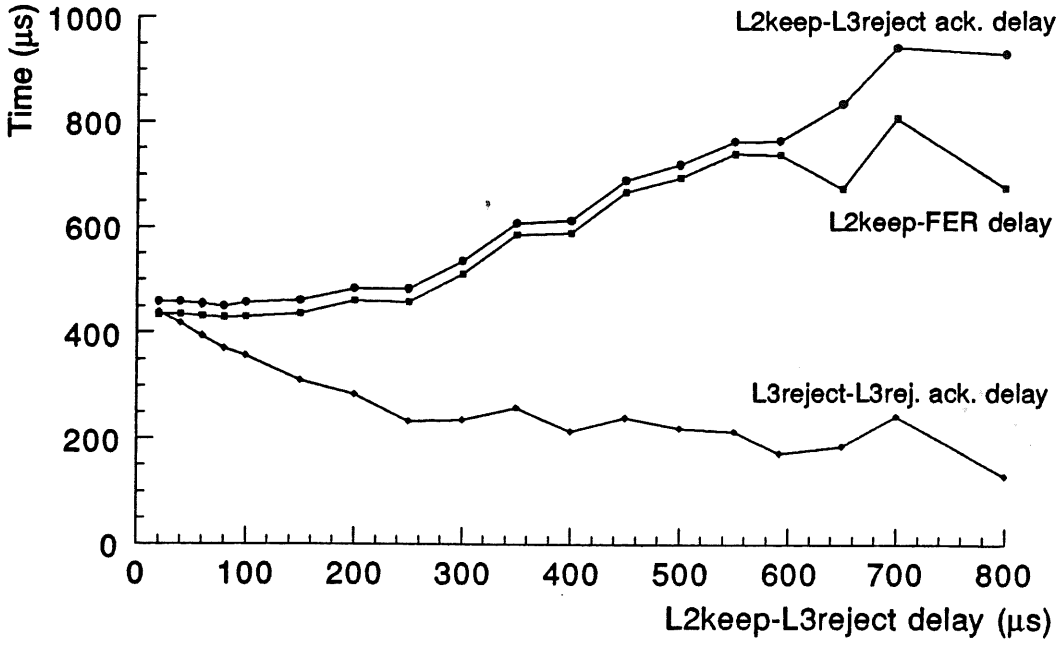


Figure 4.22: L3reject cycle acknowledgement ($Nbc = 10$)

where

- $T_{\text{FIFO}\rightarrow\text{FIC}}$ is the time required to transfer from the FIFO into the FIC all bit patterns from a given detector partition and time slice. It also includes the time used to compare each 32-bit data word with zero. This time is constant and amounts to 44 μs for the FPC and BPC branches and to 62 μs for the CPC branch .
- $T_{\text{FIC}\rightarrow\text{MEB}}$ is the time required to decode the non zero 32-bit data words and to copy from the look-up table into the MEB the channel identifiers of the non zero bits. This time is proportional to the hit multiplicity ($Nhit$).

Equation 4.4 indicates that the zero-suppression time also depends on the distribution of the non-zero bits in the data block. For instance, $T_n(Nhit = 32) \simeq 105$ μs if all hits are concentrated in a single word.$T_n = 200$ μs is obtained if they are distributed over 32 words. These numbers suggest that for large multiplicity the dominant contribution in equation 4.4 comes from $T_{\text{FIC}\rightarrow\text{MEB}}$. This is confirmed by figure 4.23 which plots the average zero suppression time $T_n = f(Nhit)$ measured with random hit distribution in the FIFO buffers. If $Nhit > 30$, the event building time is dominated by the transfers from the FIC memory into the MEB of the channel identifiers.

Equation 4.3 and figure 4.23 have been used to estimate the total event building time $(T_{\text{FIC}\rightarrow\text{MEB}})_{MWPC}$ during HERA operation (Nbc = 10). Figure 4.24

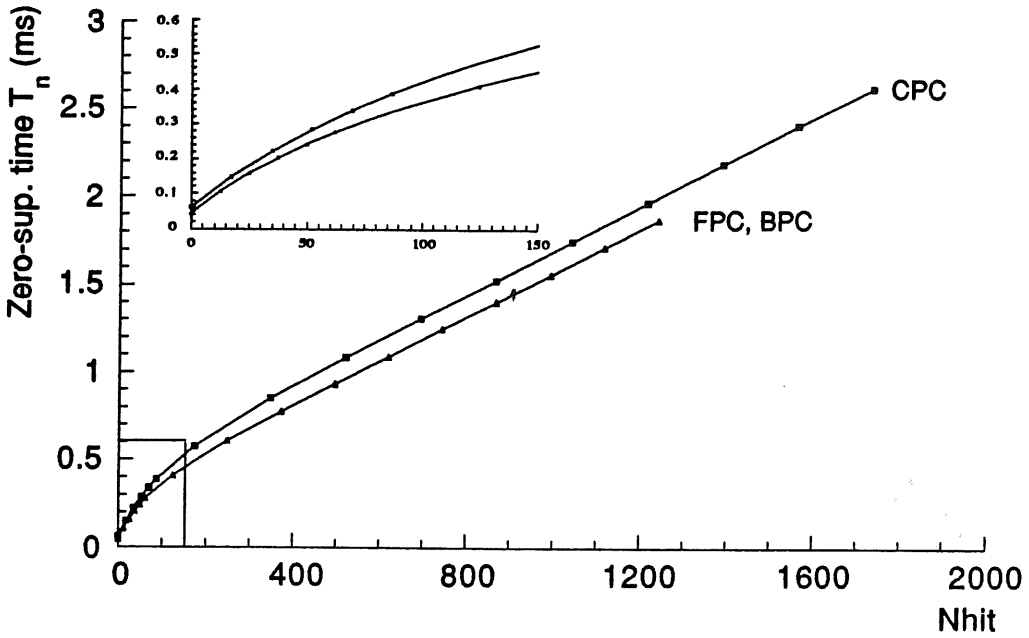


Figure 4.23: Zero-suppression time of one data block (Nbc = 1)

shows typical distributions of the hit multiplicity in the three detector partitions and the corresponding event building time. For detectors with low multiplicity (FPC, BPC), on average $\sim$ 0.6 ms per event is required to convert the raw data. For the central detectors, the average time is nearly 3 ms due to the higher hit multiplicity in the CIP and COP chambers. Very large events may require up to 13 ms. It is worth noting that these events are essentially background events not rejected by the L1 trigger system.

2. TOF data blocks

The data from the TOF counters are also transferred into the MEB after reformatting in the FIC. The off-line format chosen for the TOF BOS-banks demands intensive processing by the readout controller : $(T_{\mathrm{FIC-MEB}})_{TOF}$ varies between 70 μs and 3.7 ms depending on the hit multiplicity (for only 5 Receiver Cards !). This time could be strongly reduced if a format better adapted to the on-line constraints was used.

3. Trigger branches

The bit patterns of the Z-vertex trigger data are copied in two banks after various bit manipulations in the FIC. The processing time is constant and amounts to 47 μs per bunch crossing. The data from the forward ray finder trigger are copied directly into the MEB without formatting. This requires 44 μs per bunch crossing.

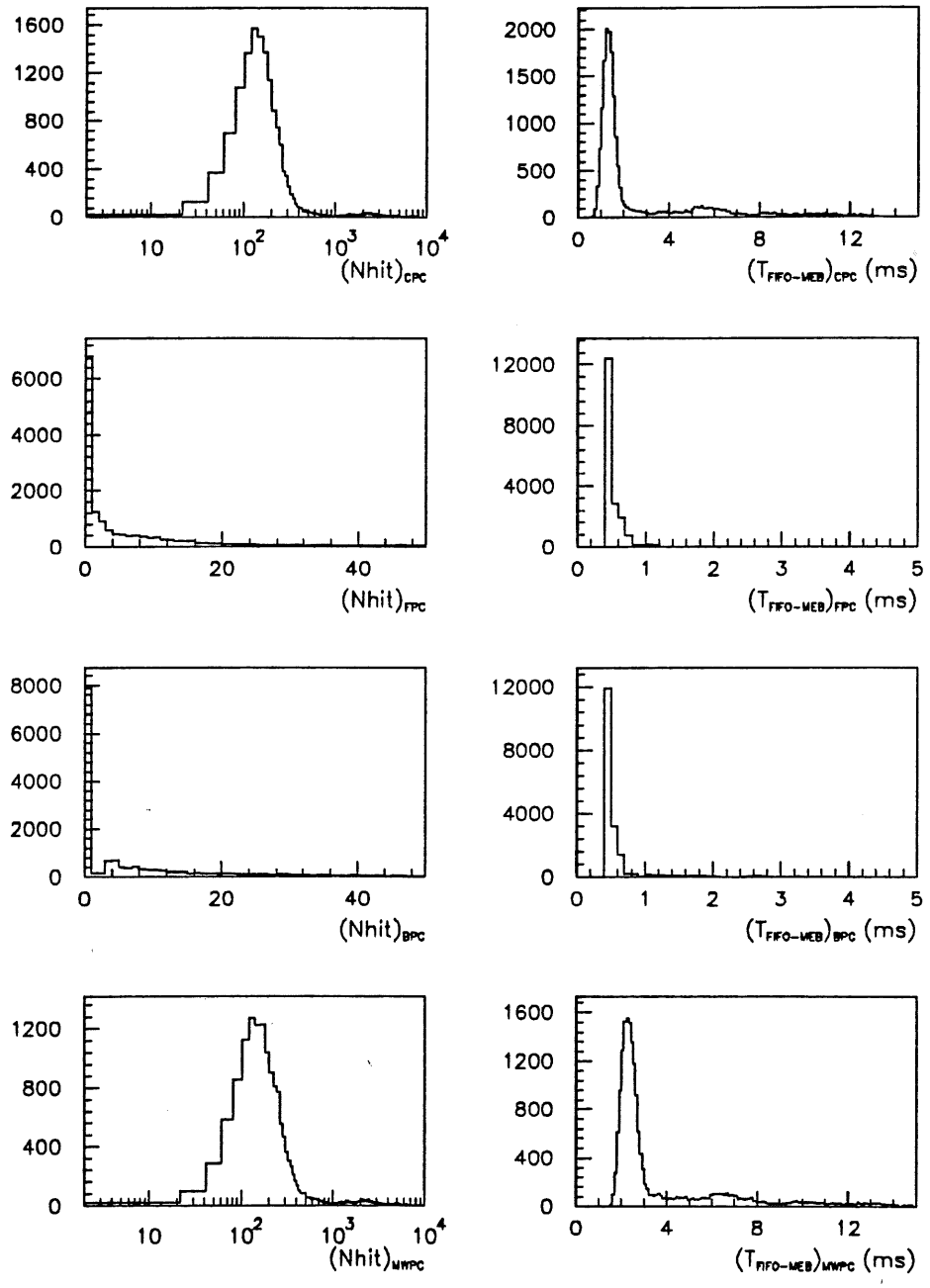


Figure 4.24: Hit multiplicity and event building time in the MWPC readout partitions

Table 4.5 summarizes the timing of the various event building processes. In total, an average time of 5.4 ms per event is needed to transfer the data from the FIFO buffers into the MEB.

Readout partition	$\overline{T}_{FIFO \rightarrow MEB}$ *(ms)*
CPC	2.82
FPC	0.52
BPC	0.60
TOF	0.5
ZVTX	0.47
FWRF	0.44
Total	5.4

Table 4.5: Event building in the MWPC readout chain (Nbc = 10)

4.9.4 Data Buffering and Dead Time Considerations

The introduction of FIFO buffers in the readout chain allows the event building task to run asynchronously from the front-end transfers. An important feature of this is that the processing of data is de-randomized and can proceed at a steady rate. Consequently, short bursts of data at high rates may be processed with small dead time losses, provided that there is enough buffer space to smooth out the statistical fluctuations in the arrival times of events. The necessary buffer depth as a function of the average trigger rates and the tolerated dead time may be estimated by studying the data flow through the system. As the process is statistical in nature, assumptions about the distributions of event arrival times and processing times must be made. Estimates can be obtained analytically for Poisson-distributed arrival and processing times [65] : a buffer depth of 3 - 5 events is sufficient to allow processing to take up to 80 - 90% of the available time without introducing large dead time, provided that the mean interval between events is not in excess of the mean processing time. For this reason, the BDC modules are equipped with 4k deep FIFO devices, providing buffer space in each branch for

$$N = INT(4096/(Nbc \sum_{i=0}^{U_n} N_i) - 1) \qquad (4.5)$$

events, in addition to the event being processed. Refer to equation 4.2 for the definition of the symbols. Table 4.6 gives the value of N for different values of

Nbc. One can see that Nbc should not exceed 10 in branch 3 and 20 in branch 4, unless deeper FIFO memories are installed.

Nbc	*Branch*					
	1	**2**	**3**	**4**	**5**	**6**
5	31	40	13	19	24	23
10	15	19	6	9	11	11
20	7	9	2	4	5	5
30	4	5	1	2	3	3

Table 4.6: Buffer length in the readout branches as function of Nbc

The conclusions obtained with an exponentially distributed processing time may be extended a posteriori to the actual processing time distribution. To show this, the data flow through the readout system has been numerically simulated using Monte Carlo methods. L2keep triggers were generated randomly using a Poisson distribution with mean rate varying from 0 to 400 Hz. The event building time was generated according to the distribution shown in figure 4.24 and the constants listed in table 4.5. Figure 4.25 shows the variation, for various values of N, of the fraction of time that the system is unable to accept new data due to a buffer full condition. The curve for an infinite buffer length is also given. In this case, no dead time is produced as long as the mean L2keep rate does not exceed $(5.4\ ms)^{-1}$, that is 185 Hz. If the L2keep rate is larger, the queue grows without limit and the system input has to be disabled periodically during some fraction of time to empty the buffers. One can readily see that a buffer capacity of $N \geq 4$ approximates closely the infinite case. For example, if $N = 6$ the dead time is reduced to 2% at 150 Hz compared to about 42% when no buffering is available.

The curves plotted in figure 4.25 correspond to runs with no L3 rejection, that is a L3keep is forced at $T_{L2} + 800\mu$s. If a certain fraction of events is rejected, the allowed L2keep rate for a given tolerable dead time increases. Figure 4.26 shows the variation of the dead time fraction for various L3reject/ L2keep ratios. These curves were calculated with the following input conditions :

- Each time a new L2keep is generated, the event building task is paused during 822μs even if this event is rejected.
- All front-end transfers in the FIFO buffers are completed, that is the raw data size is a constant.

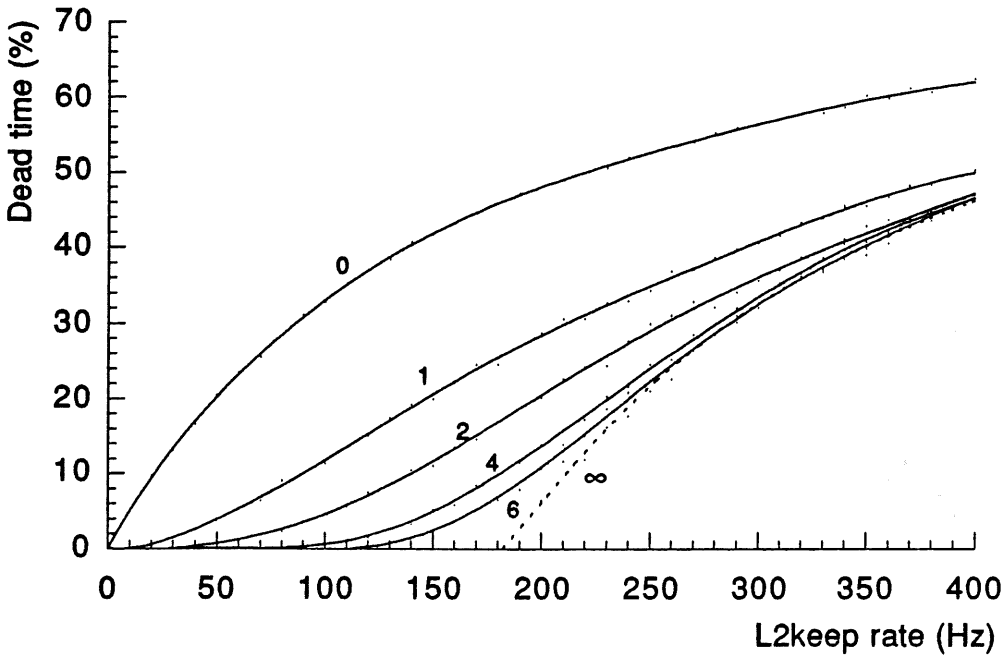


Figure 4.25: Variation of fractional dead time with L2keep rate for different values of N (no L3 rejection)

- The rejection of the L3reject data in the FIFO buffers requires a constant processing time of 200μs (25 μs per branch + overheads).

All these assumptions lead to overestimated dead time losses.

Figures 4.25 and 4.26 indicate that for L2keep rates below 200 Hz the second-order dead time is less than 10%. Introducing event rejection at the level 3 would allow to go beyond 200 Hz while keeping the dead time at a tolerable level. For instance, an event building rate (L3keep rate) of 200 Hz would produce dead time losses of between 10 and 15%, depending of the L3 rejection ratio.

4.9.5 Summary

This section summarizes the timing measurements and the results of the simulation studies.

- L3keep cycles are acknowledged in the 800 μs time window provided that the data from a maximum of 11 time slices are readout from the front-end pipelines for each triggered event.
- L3 reject cycles are acknowledged at the following times (Nbc = 10) :

$$T_{L2} + 460\ \mu s \quad \text{if} \quad T_{L3reject} < T_{L2} + 250\ \mu s \tag{4.6}$$

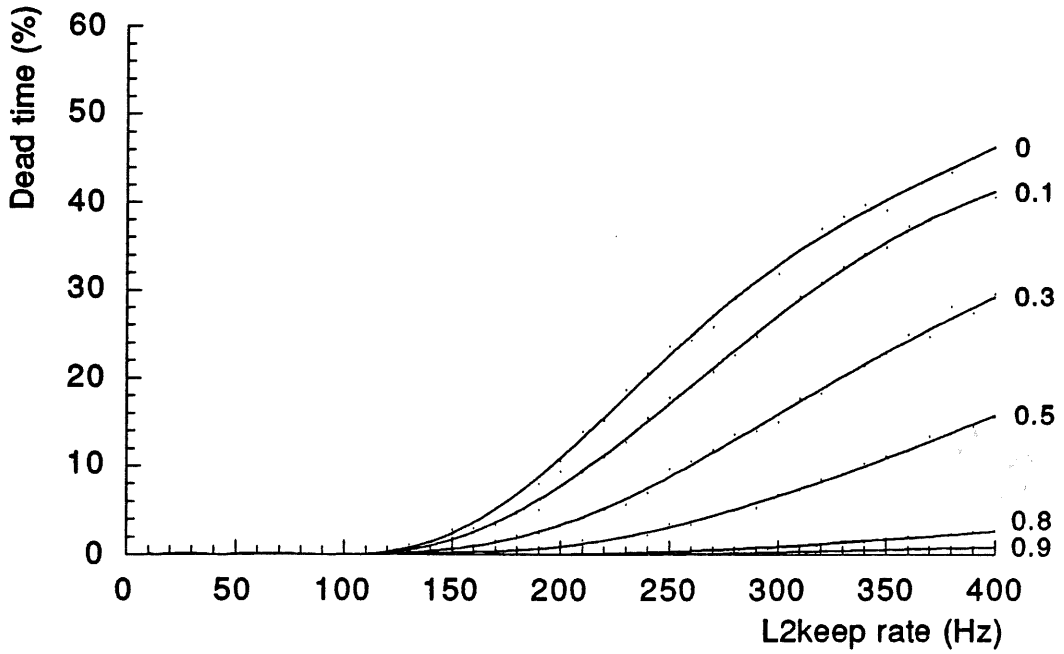


Figure 4.26: Variation of fractional dead time for various L3reject/L3keep ratios (N = 6)

$$T_{L3reject} + 220\ \mu s \quad \text{if} \quad T_{L3reject} > T_{L2} + 250\ \mu s \tag{4.7}$$

- During the 1992 operation period, the average event building time was 5.4 ms per event. This implies that with the actual buffer configuration, and in the absence of L3 rejection, L3keep rates up to 200 Hz may be sustained with less than 10% second-order dead time (1.5% at 50 Hz).
- If the L3keep rate is fixed at 200 Hz and a fraction of the event is rejected by the L3 trigger system, the dead time will be between 10% and 15%, depending on the L3 rejection ratio.

Conclusions

This thesis reports on the development and the implementation of the data acquisition system for the multiwire proportional chambers (MWPCs) and the time of flight (TOF) scintillation counters of the H1 detector at the HERA ep collider.

Four sets of MWPCs are installed in the H1 tracking system, covering nearly the full solid angle. The interaction region is surrounded by two double layers of cyclindrical chambers 2 m long and with radii of about 15 cm and 50 cm. The forward region (proton beam direction) is covered by three identical modules of planar MWPCs perpendicular to the beam axis.. The system is completed in the backward region (electron beam direction) by four MWPC planes positioned in front of an electromagnetic calorimeter (BEMC). The central and forward chambers have cathode pad readout whereas the backward chamber has wire readout. The TOF counters consist of a double wall of scintillators installed immediately behind the BEMC. The whole system of MWPCs and TOF counters totalises about 4000 electronic channels

The signals from the central and forward MWPCs are used in the first level trigger logic to reject beam-gas and beam-wall background originating outside the nominal e-p interaction region. This rejection is based on a fast (1.5 μs) reconstruction of the interaction vertex along the beam axis by a dedicated hardware logic (Z-vertex trigger). The selection of genuine ep physics events from up-stream proton beam interactions is further enhanced by time of flight measurements using the TOF counter signals. A second MWPC trigger system (forward ray finder) is implemented which identifies tracks of charged particles in the forward region. The backward MWPCs provide a space point for charged particle tracks pointing in the backward hemisphere and allows e/γ identification in the BEMC. The MWPCs form the only large solid angle sub-detector in H1 which has a charge collection time shorter than the 96 ns interval between consecutive bunch crossings. Consequently, they ensure the correct identification of the "triggering" bunch crossing.

The short time interval between bunch crossings imposes a new approach to triggering and on-line data taking. In order to have a dead time free first level trigger, pipelined processors, coupled with front-end storage devices that can accept new information every 96 ns, must be used. Successive buffering and processing stages must then be added to de-ramdomize the input data flow and to gradually identify interresting events from background data. Four levels of triggering and filtering are required to reduce the 10^7 MHz input rate to about 5 Hz at the data logging level.

Given the large number of detector components in H1, the data acquisition (DAQ) system is partionned in 12 independent front-end branches which operate in parallel. Each branch is responsible for the readout of a set of sub-detectors

(calorimeters, MWPCs,...) and consequently has its own configuration. A coherent communication protocol based on dual-ported memories and optical fibre links is used to connect these front-end systems to the central coordinating core (CDAQ) responsible for the data logging. This hierarchical structure is implemented using a common modular scheme. The IEEE 1014 VMEbus standard has been chosen to package and interconnect the electronic modules. Macintosh computers assist the tasks of program development and system supervision.

The MWPC/TOF readout branch has been developed within this framework. All front-end electronics are embedded into a dedicated open-bus communication system based around VMEbus. The analog signals from the detectors are received in 270 Receiver Cards where they are shaped, digitised and stored in a 30-stage pipeline after synchronization with the collider clock. Custom-built Controller Cards and Branch Driver Cards (BDCs) interface the 17 Receiver Card crates, grouped into 6 branches, to a central VMEbus crate. DMA controllers and FIFO buffers on the BDCs allow parallel data transfers on the branches at a rate of 4.4 Mbytes/s. Various hardware tools are provided to keep the system synchronized with the collider signals and the sequence of triggering levels. The whole system is managed by a commercial 68030-based processor board which also encodes the data in the proper format for the off-line analysis programs.

The DMA controllers handle the readout of one stage ($Nbc = 1$) in all pipelines in 64 μs. Given the software overheads, the time required to transfer the data in a typical readout configuration ($Nbc = 10$) is 660 μs. On the occurence of a transfer abort request (L3reject), the system is re-initialised in typically 220 μs. As the subsequent data processing runs asynchronously, these values determine the first-order dead time of the MWPC readout system. The second-order dead time is governed by the data encoding (zero-suppression). During the 1992 operation period, the average zero-suppression time was 5.4 ms per triggered event. Consequently,with the actual buffer configuration, the system can sustain a "trigger accept" rate (L3keep) up to 200 Hz with less than 10 % dead time (1.5 % at 50 Hz). Further improvements are expected from the use of data cache memories on the processor board.

The H1 MWPC readout system was ready in June 1992 to record the first data from collisions between 820 GeV protons - 26.7 GeV electrons. After various adjustements - bound to happen when one considers the complexity and the amount of electronics and software involved - it has performed with a high degree of reliability. This result as well as the successful operation of the whole H1 data acquisition are definitively due to the choice of exploiting the modularity and flexibility of the VMEbus standard. This architecture and the early decision of using commercial products for the processors, memories and inter-crate connections have facilitated the development of a system presently capable of coordinating the readout of 270000 electronic channels at rates greater than 50 Hz.

Bibliography

[1] R. D. Peccei, editor. *Proceedings of the Workshop on Physics at HERA.* DESY, 1987.

[2] W. Buchmüller and G. Ingelman, editor. *Proceedings of the Workshop "Physics at HERA".* DESY, 1991.

[3] B.H. Wiik. HERA : Machine and Experiment. In Springer-Verlag Berlin, editor, *Proceedings of the XXIV International Conference on High Energy Physics*, pages 404–421, 1989.

[4] B. Campbell and V. Ellias. *Canadian Journal of Physics*, 59 (1981/1972), 1981.

[5] M. Bengtsson et al. Parton Cascade Evolution Structure at HERA. In *Proceedings of the Workshop on Physics at HERA*, DESY, 1987.

[6] J. Feltesse. HERA the new frontier. In *Proceedings of the 1989 International Symposium on Lepton Interactions at High Energies*, page 13, Standford, 1989.

[7] A. Blondel and F. Jacquet. Report from the study group on detectors for charged current events. In U. Amaldi, editor, *Proceedings of the study of an e-p facility for Europe*, pages 391–394, DESY 79/438 , 1979.

[8] H. Zialepour et al. Beam hole effects on the reconstruction of kinematic variable in the H1 detector. In *Proceedings of the Workshop on Physics at HERA*, DESY, 1987.

[9] H1 Collaboration. *Technical Proposal for the H1 detector.* Technical Report, DESY, 1986.

[10] J. Bürger et al. The central jet chamber of the H1 experiment. *Nucl. Instr. and Meth.* , A279 (1989):217–222, 1989.

[11] S. Egli et al. The central-inner z-drift chamber of the H1 experiment. *Nucl. Instr. and Meth.* , A283 (1989):487–491, 1989.

[12] H. Bärwolff et al. A cylindrical z-drift chamber for H1 . In *Proceedings of the 4th Topical Seminar on Experimental Apparatus - San Miniato*, 1990.

[13] K. Müller et al. Construction and performance of a thin cylindrical multiwire proportional chamber with cathode pad readout for H1 experiment. *Nucl. Instr. and Meth.* , A312 (1992):457, 1992.

[14] G. A. Beck et al. Radial wire drift chambers for the H1 forward track detector at HERA : design, construction and performance. *Nucl. Instr. and Meth.*, A283 (1989):471–476, 1989.

[15] K. Kleinknecht. *Detectors for particle radiation.* Cambridge University Press, 1986.

[16] H. Grässler et al. Simultaneous track reconstruction and electron identification in the H1 drift chambers. *Nucl. Instr. and Meth.* , A283 (1989):622–627, 1989.

[17] R. J. Ellison. *The H1 Trigger* . H1 internal report H1-11/90-157, DESY, 1990.

[18] R. A. Eichler. Triggering with short bunch distances : the H1 trigger as an example. In World Scientific, editor, *Proceedings of the 5th International Conference on Instrumentation for Colliding Beam Physics*, pages 401–408, 1990.

[19] S. Eichenberger et al. A fast pipelined trigger for the H1 experiment based on multiwire proportional chamber signals. *Nucl. Instr. and Meth.* , A323 (1992):532–536, 1992.

[20] J. C. Bizot et al. *The first level MWPC trigger for the H1 detector.* H1 internal report H1-4/87-61, DESY, 1987.

[21] H. Krehbiel. *The H1 Trigger Decider : from trigger elements to L1keep.* H1 internal note H1-09/92-239, DESY, 1992.

[22] J. Fent et al. *A Level 2 Calorimeter Trigger Using Neural Networks.* H1 internal note H1-04/91-172, DESY, 1991.

[23] W. J. Haynes. *Experiences at HERA with the H1 Data Acquisition System.* Technical Report 92-129, DESY, 1992.

[24] *VMEbus Specification Manual.* Revision C.1. edition, 1985.

[25] *The VME Subsystem Bus (VSB) Specification.* Revision A.1. edition, 1986.

[26] S. Kolya. *H1 drift chamber data acquisition system.* Technical Report not published, DESY, 1992.

[27] W. Zimmerman et al. *A 16 channel VME Flash ADC system.* Technical Report not published, DESY, 1989.

[28] P. Robmann et al. Construction and analysis of a prototype drift chamber for the H1 experiment. *Nucl. Instr. and Meth.* , A277 (1989):368–378, 1989.

[29] H. Brettel et al. *The Electronic System for the H1 Liquid Argon Calorimeter.* H1 internal report H1-TR–115, DESY, 1987.

[30] M. Djidi. *DSP readout of ADCs for the H1 calorimeter.* H1 internal note H1-10/90-155, DESY, 1990.

[31] F. Descamps. Embedded DSP and RISC processors for H1 calorimeters acquisition. In *First Annual Conference on Electronics For Future Colliders*, pages 119–126, LeCroy Corporation, 1991.

[32] E. Pietarinen. A VME Data Acquisition Processor with Fiber Optic Links. In North-Holland, editor, *Proceedings of the VMEbus in Research Conference*, pages 133–137, 1988.

[33] *TAXIchip Integrated Circuits, Technical Manual.* Advanced Micro Devices, 1989.

[34] Alan J. Campbell. *A RISC Multiprocessor Event Trigger for the Data Acquisition System of the H1 Experiment at HERA.* Technical Report RAL-91-060, RAL, 1991.

[35] B. G. Taylor. MICRON: VMEbus and CAMAC access from the Macintosh II. In North-Holland, editor, *Proceedings of the VMEbus in Research Conference*, pages 257–264, 1988.

[36] M. Demoulin. *VMEUA1MON Users Manual.* CERN-EF-UA1, 1988.

[37] *MPW Reference Manual 5.* Apple Developers Group, ADG 1987/8 edition.

[38] W. J. Haynes. *VMEbus Interactions from the MPW Shell.* DESY, Version 3.0 edition, 1992.

[39] F. Sauli. *Principles of Operation of Multiwire Proportional and Drift Chambers.* Technical Report CERN 77–09, CERN, 1977.

[40] I. Endo et al. Systematic shifts of evaluated charge centroid for the cathode read-out multiwire proportional chamber. *Nucl. Instr. and Meth.* , A188 (1981):51–58, 1989.

[41] G. Battistoni et al. Resistive cathode transparency. *Nucl. Instr. and Meth.*, A202 (1982):459–464, 1982.

[42] Peter Rice - Evans. *Spark, Streamer, Proportional and Drift Chambers.* The Richelieu Press, London, 1974.

[43] V. Radeka. Low-noise Techniques in Detectors. *Ann. Rev. Nucl. Part. Sci.*, 38:217–277, 1988.

[44] A. Hrisoro and G. Martin. *The Preamplifier and Shaping Amplifier of the H1 MWPCs.* Technical Report, LAL, 1993. Not published.

[45] A. Hrisoro. Time domain noise calculation for the common base current amplifier configuration. *Nucl. Instr. and Meth.* , A185 (1981):207–213, 1981.

[46] H. Krehbiel. *MWPC Receiver Card; semi-final circuit diagram.* H1 internal note MWPC n^{0}5, DESY, 1988.

[47] H. Riege and R. van Staa. *H1 muon detector : digital front-end electronic.* H1 internal report H1-TR 400, DESY, 1987.

[48] H. Krehbiel. *A Memo about the Sync Gate Array in H1 MWPC Circuits.* H1 internal note H1 MWPC Note n^0 4, DESY, 1988.

[49] P. Huet. *The Branch Driver Card.* IIHE, July 1993.

[50] *MC68450 Technical Data.* Motorola Inc., 1986.

[51] H. Krehbiel. *The H1 Trigger Control System.* H1 Trigger note Note n^{0}11, DESY, 1988.

[52] *VMEbus Repeater Link Model VMIVME - Repeat L.* VMIV USA, 1992.

[53] H. Krehbiel. *The Fast Card of the Subsystem Trigger Contoller.* H1 technical report, DESY, 1990.

[54] J. Olszowska. *The Slow Card of the Subsystem Trigger Contoller.* H1 technical report, DESY, 1991.

[55] H. Krehbiel. *The Fanout Card of the Subsystem Trigger Contoller.* H1 technical report, DESY, 1989.

[56] H. Krehbiel. *The Extended Fanout Card of the H1 STC.* H1 technical report, DESY, 1991.

[57] H. Krehbiel. *The Triggerbits Card of the H1 STC.* H1 technical report, DESY, 1992.

[58] *Fast Intelligent Controller FIC 8230/8232.* Creative Electronic System SA, Geneva, CH. 1987/199.

[59] *DPM8242.* Creative Electronic Systems SA, Geneva, CH, 1989.

[60] *SYS68K/RR-2.* Force Computers Inc, Campbell,USA, 1991.

[61] *SYS68K/DRAM-8.* Force Computers Inc, Campbell,USA, 1991.

[62] *VMVbus one Slot VIC8250 Users' Manual V.2.1.* CES CH, 1991.

[63] J. Moreels. *The H1 MWPC Data Acquisition Software.* to be published.

[64] W. J. Haynes. *VMEXI - SSP : VMEtaxi System Software Package.* DESY, Version 3.9 edition, June 1992.

[65] G.P. Heath. Dead time due to trigger processing in a data acquisition system with multiple event buffering. *Nucl. Instr. and Meth.* , A278 (1989):431–435, 1989.