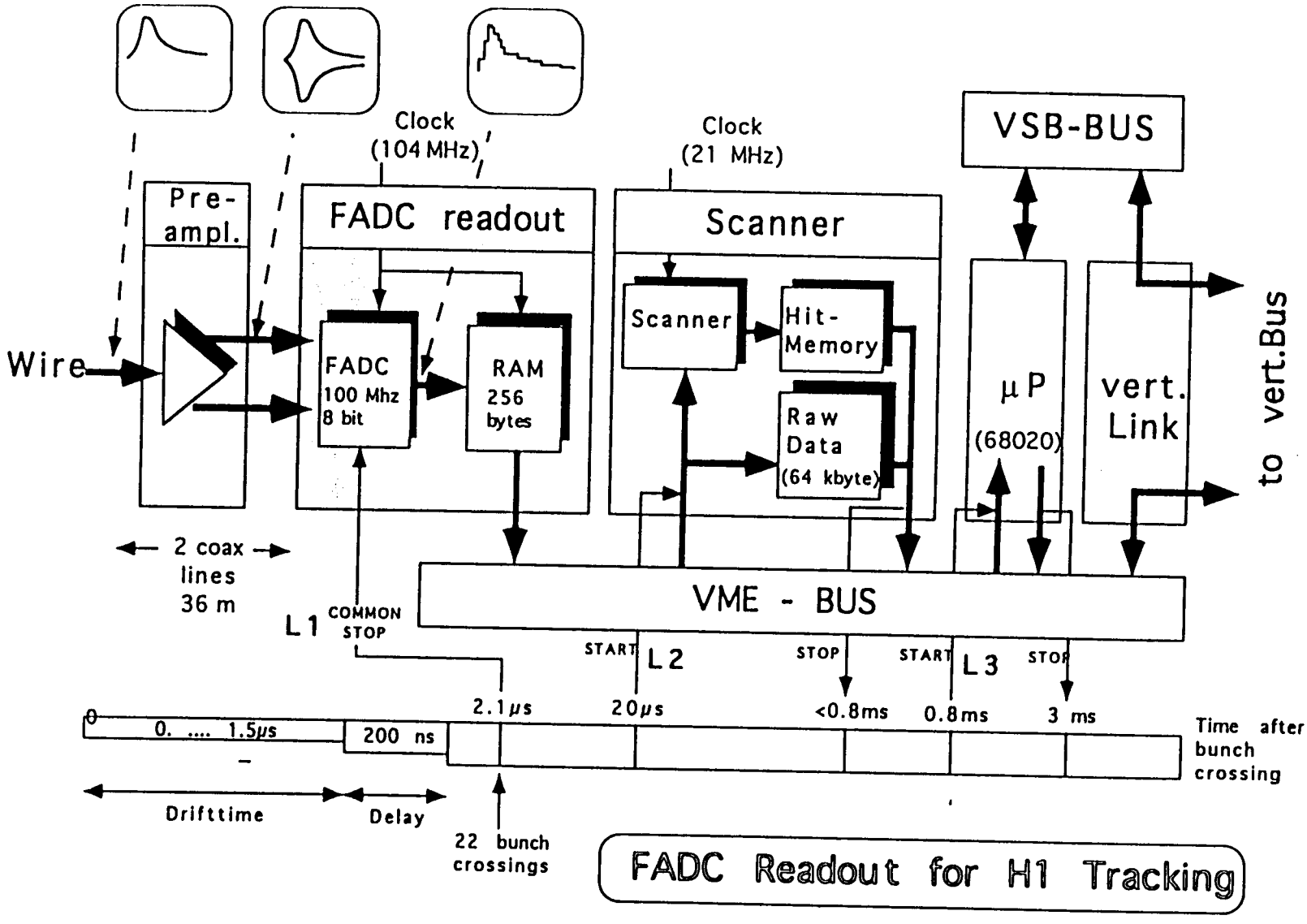
Clock
(104 MHz)
Clock
(21 MHz)
VSB-BUS
Pre-
ampl.
FADC readout
Scanner
Wire
FADC
100 Mhz
8 bit
RAM
256
bytes
Scanner
Hit-
Memory
Raw
Data
(64 kbyte)
µP
(68020)
vert.
Link
to vert.Bus
2 coax
lines
36 m
VME - BUS
L1
COMMON
STOP
START
L2
STOP
START
L3
STOP
2.1µs
20µs
<0.8ms
0.8ms
3 ms
0
0. .... 1.5µs
200 ns
Time after
bunch
crossing
Drifttime
Delay
22 bunch
crossings
FADC Readout for H1 Tracking