and the ionization collection efficiency on the first sense wire is optimal right to the edge of the gas volume.

Because all the sense wires are in the radial direction, a coarse determination of the radial position of a track may be made from charge division if a wire is read out at both ends. However it is not physically possible to have preamplifier cards at the small radius end. For this reason the sense wires of one 7.5° sector drift cell are connected at the inner hub to the sense wires of another 7.5° sector drift cell, actually 105° away in azimuth, so that when sense wires are read out at the outer radius charge division is possible along this double length of radial wire. Current sensitive preamplifiers are at each end of these sense wire pairs, each channel of which drives approximately 40 m of cable to the FADC system. Pulse profile (Q, t) analysis gives the drift coordinate perpendicular to the sense wire plane, and two pulse integral measurements Q_L and Q_R from the two ends give the radial position by charge division.

The spacing in the z direction between the sense wires of the radial chambers, between the three modules, and the sets of planar drift chambers and the radial drift chambers may be seen from Table 3. Concerning the azimuthal position of the radial chambers, the plane which bisects a 7.5° sector cell (and about which the sense wires are staggered) is at $\phi = 3.75°$ in the first module, at $\phi = 7.5°$ in the second module and at $\phi = 6.25°$ in the third module. The resolution achieved with the 50 % argon, 50 % ethane gas mixture used so far is $150 - 200$ μm. The gas mixture which is intended to use for optimal detection of transition radiation is given in the following section.

2.3.3 Transition radiators

A passive array of polypropylene layers provides a sufficient number of dielectric interfaces for useful transition radiation (TR) X-ray emission. The dielectric constant, the layer thickness and the mark to space ratio of the polypropylene sheets determine the X-ray yield and the energy spectrum. For the values chosen the spectrum peaks around 6 keV for 20 GeV electrons. The interface between the TR and the radial wire drift chambers has been optimised for transmission of these X-rays. As described in the previous section the radial wire drift chambers are designed and operated both for optimal track point measurement and efficient X-ray detection. The combination of TR and radial wire drift chamber is designed for electron-pion discrimination, at the level of 90% electron acceptance with less than 10% pion contamination, up to 80 GeV for tracks passing through all three modules of the FTD. To achieve this, it is planned to operate the radial wire chambers with a gas containing xenon which has a high photoionization cross-section at 6 keV. A 20 % xenon, 40 % helium, 40 % ethane mixture satisfies the requirements of TR detection with acceptable charged track dE/dx ionization density, and also suitable drift velocity for the requirements of the drift chamber. Data taken with a radial drift chamber in a test beam at CERN have shown that the design discrimination between electrons and pions can be achieved with this gas [28, 29].

The assembly of polypropylene sheets is self supporting but is enclosed in its own gas envelope in order to isolate it from the gases used in the rest of the FTD. The helium-ethane mixture surrounding the polypropylene sheets is chosen to give the same partial pressure of helium as in the radial drift chamber. This is important because the interface is the thin mylar TR window of the radial drift chamber section which could be damaged by pressure differences in excess of about 100 μbar.

2.4 Drift chamber electronics, readout, and front end data processing

2.4.1 Introduction

All drift chambers in H1 are connected to one of the three independent branches of the central data acquisition system (CDAQ). The analog signals are digitized and processed in a number of

Chamber	Branch #	# of crates	# of channels	Raw data [Kbyte]	(Q,t) data [Kbyte]
Radial	5	9	1728	20.5	2.4
Planar	5	6	1152	28.5	4.1
CJC1 and CJC2	4	23	2640	33.2	5.4
COZ	4	1	96	3.41	0.5
CIZ	4	1	60	5.14	0.9
Forward muons θ	6	4	1024		

Table 4: Summary of drift chamber readout data.

front end crates, the trigger connection is based on the H1 standard subsystem trigger controller crate and interface cards and local logic produces and distributes control signals to the front end crates. A master crate collects the complete data from the branch and sends it to the CDAQ. Crates for local data monitoring can be added. Figure 11 shows the general layout of each drift chamber branch.

The drift chambers are distributed between the branches according to position in the detector. The inner and outer jet chambers and the inner and outer z chambers form branch 4 (CTD). The forward radial and planar chambers form branch 5 (FTD). The $\theta-$ and $\phi-$ chambers of the forward muon spectrometer form branch 6 (FMu). Table 4 shows the sizes of the various components, and the typical size of the zero suppressed digitizations (raw data) and processed summary data ((Q,t) data).

2.4.2 Operation of the readout

The analog signals from the preamplifiers mounted on the detector are received by 104 MHz FADC cards which continually digitize and store the data - at this point we are recording data at a rate of over 600 Gbyte/s over all drift chambers. On receipt of a first level trigger (L1) signal the digitization is stopped so that the data recorded in the FADC card memory includes, for each detector, all digitizations which could have occured between the time of the event and the maximum possible drift time for that chamber.

At a second level trigger (L2) signal the full 2.5 Mbytes of raw data for an event is copied by the scanner controller cards into the second level buffer at a speed of 3.3 Gbyte/s. At a third level trigger (L3) signal, the processor card in the FADC crate reads the data from the scanner, and writes an off-line format data bank into an intermediate buffer which contains blocks of significant, zero suppressed data with an event size of approximately 100 Kbyte. The output is written into a triple ported buffer memory on the intercrate connection (VIC8251 [30]). When a complete event is available from all front end crates the master processor collects the data from this buffer memory and writes the complete event to the multi-event buffer of the optical fiber VMEtaxi link (see Section 7.1.2 of reference [1]).

2.4.3 Amplifier and FADC

The sense wires of the tracking drift chambers are connected to amplifiers either at one or at both wire ends. The eight-channel amplifier cards are mounted directly on the chamber vessel. The sense wire and the grounded potential wires serve as differential input. The sense wire is at positive HV and therefore it is coupled to the amplifier via a capacitor (1.5 nF). The sense wires (in some chambers) and amplifier are protected by a spark gap, and a pair of crossed diodes to ground. Each amplifier channel consists of two stages of video amplifiers. The amplification is large enough so that no further amplification is needed on the readout card. This gives optimum noise rejection and minimises the influence of pick-up on the cable to the readout card. The amplifier card has two test inputs which allow the application of test pulse signals to the inputs of odd or even amplifier channels.

The 9520 signals from the drift chamber are digitized by F1001-FADCs [31]. The sampling frequency is 104 MHz, generated by an oscillator phase locked to the bunch crossing clock of the HERA storage ring of 10.4 MHz. The differential outputs of the amplifiers are connected to the FADC cards with multi-coaxial cable of about 28 m length. This cable also carries the power and test lines to the preamplifiers. The FADC-chips used have a resolution of eight bits [31]. The combined signal is fed to the FADC chip through a transformer eliminating DC offsets and via a resistor network that includes feedback of the input signal to the voltage reference, providing a non linear response with 8 bit accuracy for small signal amplitudes and a 10 bit dynamic range. Each FADC-chip is connected to one 256 byte deep memory which serves as circular buffer. During the active sampling phase of the FADC system signals are continuously digitized and stored in the memories. This recording process is stopped by a trigger signal that freezes the history over 2.5 μs in the memory. Sixteen FADC-channels are housed on one F1001-card and up to 16 F1001 cards are housed in a F1000 crate. It has a VME backplane used for fast 32-bit wide readout of the digitized signals from the FADC-memories. The signal risetime at the sense wire is a few ns. It is deliberately degraded by the amplifier band width, cables, and coupling transformer to 18 ns (20 % to 80 % of pulse amplitude) at the input of the digitizing FADC. This is the optimum for a time measurement with a FADC sampling at 100 MHz.

2.4.4 The scanner and the front end processor

In each F1000 front end crate there is an M1070 scanner card that acts as a sample controller for the FADCs, and provides fast readout and zero suppression of the FADC data. The scanner supplies the 104 MHz clock to the FADC cards, and at a L1 trigger gates this clock such that the circular buffers of the F1001 cards contain the required time segment. At a L2 trigger signal it copies the data from the FADCs into a local buffer in a series of synchronous bursts over the VME bus, in this way a transfer speed of 80 Mbyte/s is achieved, and the data for a full crate can be copied within the 800 μs requirement of H1. During the copy the data is compared with programmable thresholds and any significant transition (presently two subsequent time bins above or below threshold) is recorded in the hit table.

At a L3 trigger signal the scanner interrupts the front end processor (24 MHz FIC 8231 [32]) present in each F1000 crate. The interrupt handler reads the hit table from the scanner, calculates the required blocks of raw data, and copies these blocks into a multievent raw data buffer in an off-line format data bank. Each block includes four pre-samples before the hit starts to allow dynamic calculation of the pedestal, and blocks are merged in cases where a block would influence a subsequent block on the same wire. An output bank is written into a multievent output buffer in the memory of the VIC 8251 interconnect card, using the VSB bus connecting the processor and the interconnect, since the VME bus may be occupied by the scanner reading a subsequent event. The input raw buffer and output buffer both typically hold 30–40 events, and this allows derandomization over many events of the large range in processing times caused by localised high track density.

2.4.5 Determination of charge and time (Q, t)

The relevant parameters of a signal pulse from a drift chamber wire are signal timing (t) and the pulse integral (Q). These signal parameters are determined by a program which runs on the

L4 farm (see Section 5.5 of reference [1]). In this way the amount of raw data is reduced by a factor of about five. The zero suppressed data provided by the scanner are treated in several steps. For the CJC, CIZ, COZ and the radial chambers the first three steps consider the data of both wire ends separately, while the further steps use the combined information.

In the $(Q, t)-$algorithm the FADC data are first linearised. The leading edge of a new pulse is found by a search for a maximum in the difference of successive samples above the threshold. The average of the six digitizations before the pulse start is used to evaluate the pedestal to be subtracted from the pulse. Hits from the two ends of a wire are combined if the leading edges differ by less than or equal to two clock bins.

The essential information for the drift time determination comes from those electrons which arrive first at the sense wire and which are produced along the track in the region tangential to the isochrones. These electrons contribute to the sharp rise of the pulse, which is, however, smeared out by diffusion, chamber capacity, and amplifying electronics. The remaining off-tangential electrons arrive at later times and fluctuations of their ionization density influence only the trailing edge of the pulse, otherwise determined by the differentiating electronics.

The drift time is determined by chamber specific algorithms. For the CJC e.g., the time at half the full amplitude is determined by linear interpolation, averaged over both wire ends and used with the average risetime to extrapolate to the arrival time of the first electrons, taken at 10 % of the pulse amplitude. The average pulse consists of about 20 digitizations, while 10.4 MHz noise pulses extend typically over 5 bins and can therefore partly be rejected at the scanner level. The pulse integral is determined by summing some fraction of these digitizations. Most important for the CJC (and radial drift chambers) is the relative error of the integral for the $z(r)$ determination. It is minimised by choosing a rather short integration interval of eight time bins. The timings of the pulses from the two wire ends differ because of different cable length and signal propagation along the wire. Therefore the phase of the integration interval has to be properly adjusted in order to guarantee the integration over the same part of the pulse on both wire ends.

If a pulse is recognized on the tail of a previous one it is analysed after effects from the previous pulse have been subtracted on the two wire ends independently. For this subtraction a standard pulse shape is determined by averaging a large number of pulses, and then matched in phase and normalised in height to the preceding pulse.

2.4.6 Implementation

The subsystem trigger controller crate (STC, [33]) provides a standard interface to the central trigger electronics (see also section 5.3.5 of reference [1]). The STC in the DC readout is supplemented by a 104 MHz phase locked loop (PLL) card providing an accurate (± 1 ns) clock and a logic card acting as sequence controller. Although responses from the scanner could by simple combination be used directly to respond to the central trigger, inclusion of the logic card in the path allows better overall performance by overlapping some stages of processing with refill and other delays of subsequent events. This places much of the response time of the DC systems in second or even third order dead time, and allows the DC systems to be run at almost full throughput with little or no actual dead time.

The master crate contains interfaces to the CDAQ (VMEtaxi link) and to other crates in that branch (VIC8251) consistent with the common H1 architecture (see Section 7.2.1 of reference [1]). On startup, the master processor loads all other processors with code and data stored in non volatile ram. Once the other processors are running, all communication is made through the buffer memory of the VIC boards connected to each of the remote processors. During a run the master processor operates asynchronously, waiting for an event to be signalled by the trigger processor, and then polling the front end processors until the complete event is ready to be built. The events are not buffered or processed by the master processor.

A monitoring crate provides access to the readout branch for chamber specific control and monitoring systems. A small fraction of the event data can be passed to the monitoring crate for local monitoring, especially that which requires raw data that might be unavailable in the CDAQ monitoring systems. Data is collected from a dedicated memory in the master crate using a differential VSB extension [34] – the VIC8251 connection is not used for technical reasons. Data may also be fed back from the monitoring system into the data stream, to allow important slow control information (e.g. HV, currents) to be recorded together with the event.

The drift chamber readout uses processors of the Motorola 68000 family throughout. These CISC processors are relatively easily programmed at the native instruction level, and all the readout code was written in assembler. By splitting the workload between many processors each fulfilling a specific task it has been possible to avoid the use of an operating system on any of the readout processors. This has minimised response times and maximised performance.

2.5 Proportional chambers

Between 5° and 175° the solid angle seen from the interaction region is completely covered by multiwire proportional chambers. Six independent planes in the forward direction, four in the central and also in the backward direction serve three different functions: to deliver a fast timing signal with a time resolution better than the separation of two succeeding HERA bunch crossings, to provide moderately accurate space points for charged particle track reconstruction at the first level trigger and lastly to add an accurate track element in the backward direction, where the drift chambers fail to provide enough space points.

The planar forward chambers (FWPC) are interspaced between the driftchambers of the FTD described above and are exposed to high particle rates increasing towards the beam pipe. Hence minimum overall thickness and minimal amount of material traversed, sufficient ageing prospects, and cathode pad size adapted to increasing rates near the beam pipe became the primary design criteria. These points do also apply for the two cylindrical chambers in the central region. The inner one (CIP) is closest to the interaction region and covers the largest solid angle. In order not to degrade the track reconstruction of the surrounding drift chambers, the CIP and its outer partner (COP), were fabricated with low mass materials and a narrow active gap. Since the main purpose of the FWPC, COP and CIP is to provide space points for the first level trigger, a pad segmented cathode readout was chosen with graphited surfaces as in other chambers built for high rates [35, 36]. From the reconstructed tracks the event vertex can be deduced and other detector data such as calorimeter and muon information can be validated. Since the trigger logic requests three space points per track, spurious background hits from uncorrelated noise and synchrotron radiation are removed.

In the backward direction the reconstruction of the scattered electron in low momentum transfer events calls for an accurate track segment. This is given by the signals from the four differently oriented anode wire planes of the backward chamber (BWPC). Several wires can be combined for triggering purposes. Standard planar chamber construction techniques sufficed here, since more than one radiation length of electronics and cables from the central tracker separate the BWPC from the interaction region. The BWPC covers the front surface of the backward electromagnetic calorimeter (BEMC) and hence also serves to discriminate electrons and photons.

The properties of all four chamber types are summarized in Table 5. The front end electronics and readout system is identical for all chambers.