Programming the H1 CST Decoder Chip

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Introduction

The H1 CST decoder chip was developed at the Paul–Scherrer–Insitute and the Institute for Particle Physics of the Swiss Federal Institute of Technology in Zurich (ETH Zürich).

Two versions exist:

- The chip SAC1 PSI21, fabricated in SACMOS1 technology, developed in 1994 (see Fig. **??**).
- The prototype chip DMILL PSI39, fabricated in radiation hard DMILL technology, developed in 1999 (see Fig. **??**).

The DMILL PSI39 chip was designed to be as compatible to the SAC1 PSI21 chip as possible.

Input Signals

The chip is operated mainly by four digital input signals, which are fed into differential inputs:

- OUT/$\overline{\text{SR}}$ is a switch between output (OUT/$\overline{\text{SR}}$ = 1) and shift register (OUT/$\overline{\text{SR}}$ = 0) mode.
- CLK1 is the first clock signal.
- CLK2 is the second clock signal.
- BIN is the binary input signal.

CLK1 and CLK2 are normally operated as a two–phase clock; in normal operation, a clock cycle consists of the following sequence:

CLK1	CLK2
0	0
1	0
0	0
0	1

In normal operation, CLK1 and CLK2 are never in a “1” state at the same time.

Additionally, there exists an input signal RBE (Read Bit Enable), which is relevant in **readout mode** (see below).

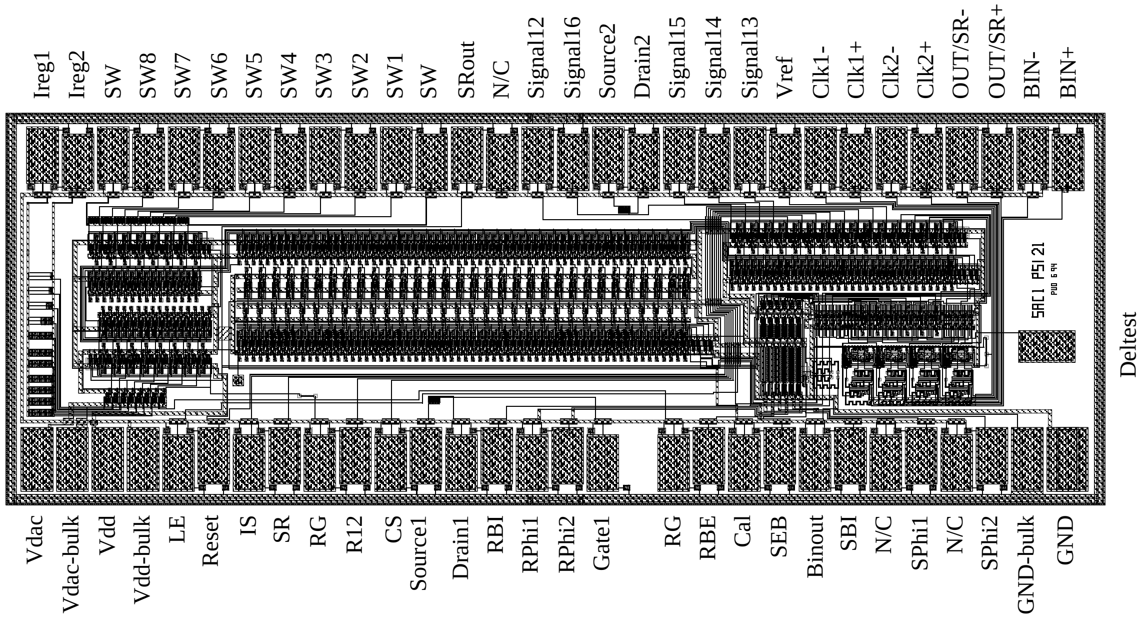

Figure 1: Layout of the SACMOS1 PSI21 decoder chip.

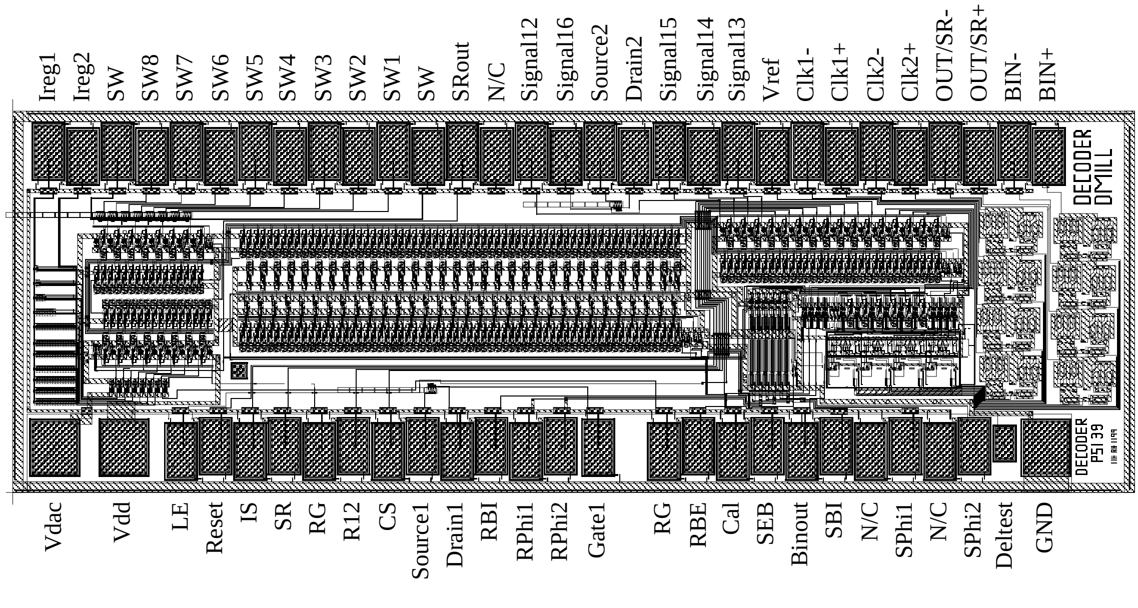

Figure 2: Layout of the DMILL PSI39 prototype decoder chip.

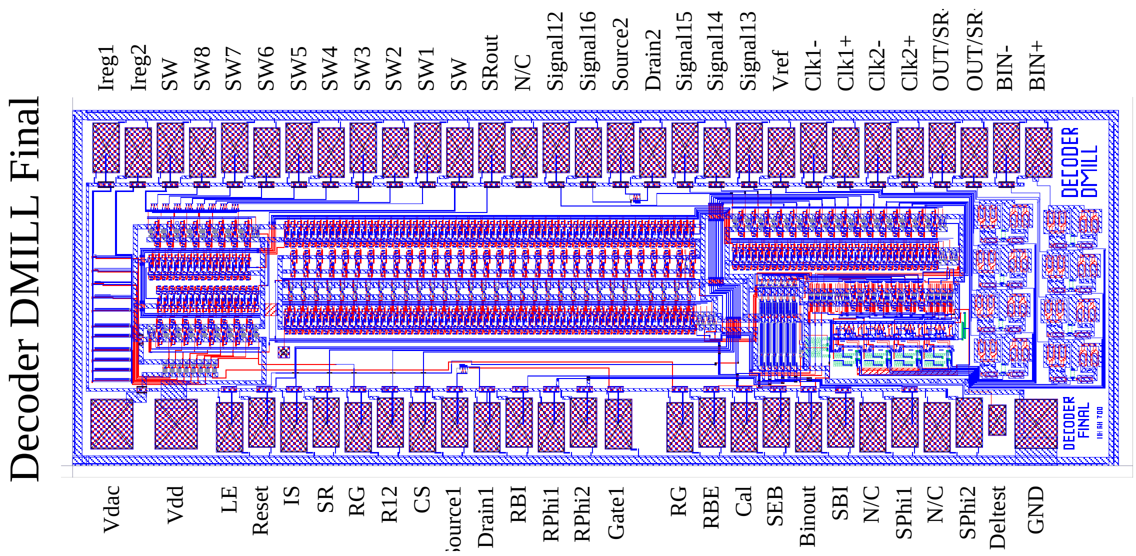

Figure 3: Layout of the final DMILL decoder chip.

The $\mathrm{OUT}/\overline{\mathrm{SR}}$ Signal

The chip has two main modes of operation, which are selected by the $\mathrm{OUT}/\overline{\mathrm{SR}}$ signal:

- The **output mode** ($\mathrm{OUT}/\overline{\mathrm{SR}} = 1$).
- The **shift register mode** ($\mathrm{OUT}/\overline{\mathrm{SR}} = 0$).

The Shift Register Mode

In shift register mode, the signals CLK1, CLK2 and BIN are used to load a 64 bit shift register.

This shift register is actually a sequence of four shift registers:

- A 16–bit shift register that feeds the **APC signals register**.
- A 32–bit shift register that feeds the **calibrate register**.
- A 8–bit shift register that feeds the **control register**.
- A second 8–bit shift register that feeds the **current supply register**.

These four shift registers are chained together to form a single 64–bit shift register.

In shift register mode, the BIN signal is fed into the input of the shift register, and for each clock cycle one bit is put into the shift register. Therefore 64 clock cycles are needed to completely fill the shift register (SR); after these 64 clock cycles, the first bit fed into the SR will appear as bit 64 of the SR, the second bit as bit 63, and so on.

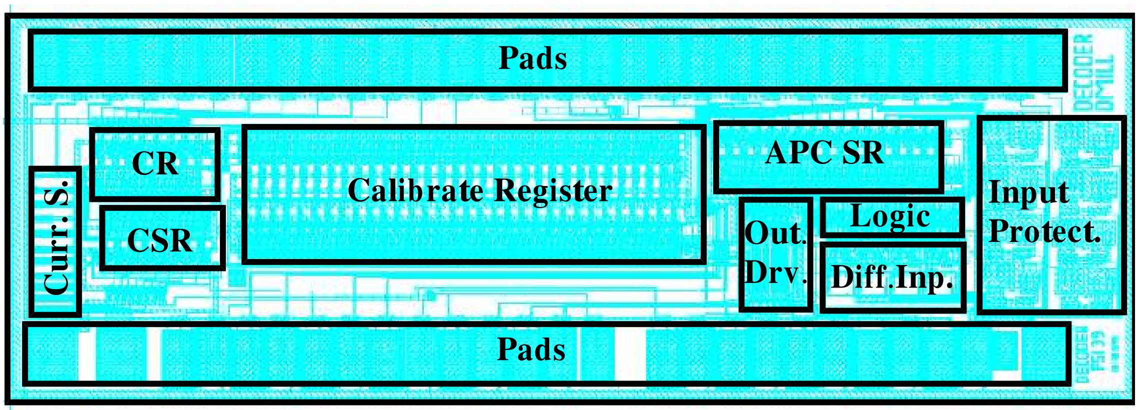

Figure 4: Overview over the function blocks of the DMILL PSI39 prototype decoder chip.
The abbrevations stand for: **APC SR**: APC signals register; **Curr. S.**: current source; **CR**: control register; **CSR**: current supply register; **Out. Drv.**: output drivers (for the signals SBI, SPhi1, SPhi2, RBI, RPhi1, and RPhi2) **Diff. Inp.**: differential inputs; **Input Protect.**: input protections.

As explained above, the four shift registers are connected to buffer registers (the APC signal, calibrate, control and current supply registers). In shift register mode, these registers are decoupled from the shift register, so that their output is stable while the SR is filled.

After the shift register has been filled, the OUT/$\overline{\text{SR}}$ signal will go back to 1, putting the chip into **output mode**.

At this point, the 16 bits from the first 16–bit shift register are transferred into the APC control register.

After this has been done, three of the *newly set* first four bits of the **APC signals register** determine which, if any, of the other three latch registers are updated from the corresponding shift registers:

- **Bit 2** steers the transfer to the **calibrate register**.
- **Bit 3** steers the transfer to the **control register**.
- **Bit 4** steers the transfer to the **current supply register**.

Therefore it is possible to use

- **16 clock cycles** to just update the **APC signals register**, in which case bits 2, 3, and 4 must be set to 1 (0 means “transfer”),
- **48 clock cycles** to update the **APC signals register** and the **calibrate register**, in which case bit 2 must be set to 0, and bits 3 and 4 must be set to 1,
- **56 clock cycles** to update the **APC signals register**, **calibrate register**, and the **control register**, in which case bits 2 and 3 must be set to 0, and bit 4 must be set to 1,

- and **64 clock cycles** to update the **APC signals register**, **calibrate register**, **control register**, and the **current supply register**, in which case bits 2, 3, and 4 must be set to 0.

Note: When one uses the H1CPG program, filling of the shift register is done with the command `MOVn`, where n is either 2 (= 2×8 bits), 6, 7, or 8.

Therefore these commands should only be used in the following way:

```
MOV2 ?111 ???? ???? ????
MOV6 ??11 ???? ???? ???? x????????
MOV7 ???1 ???? ???? ???? x???????? x????
MOV8 ???? ???? ???? ???? x???????? x???? x????
```

A complete filling sequence will always have the commands `SR` before and `OUT` after the `MOVn` command.

Fast Reset of the Shift Register

Internally the shift register consists of 128 storage cells which are connected by transmission gates; these transmission gates are alternatingly connected to the PHI1 and PHI2 signals (which in shift register mode are connected to CLK1 and CLK2, respectively).

If CLK1 and CLK2 are 1 at the same time, all transmission gates are open, so that any signal on BIN is immediately (apart from the delay of the signal in the various transistors) transmitted to all cells in the shift register. This can be used to reset the chip very fast with the following sequence:

OUT/$\overline{\text{SR}}$	CLK1	CLK2	BIN	Remark
0	1	1	0	Set all bits in the shift register to 0
0	0	0	0	Close transmission gates
1	0	0	0	Go to output mode

(Actually, the "close transmission gates" phase is not strictly necessary.) Since all bits, including bits 2, 3, and 4 of the APC signals register are set to 0, also the calibrate, control and current supply registers are reset at the moment when OUT/$\overline{\text{SR}}$ goes to 1.

Since bit 1 of the APC signals register is set to 0, the chip will be in readout mode after this fast reset.

The Output Mode

In output mode (OUT/$\overline{\text{SR}} = 1$, the shift register and the latch registers are in a stable state.

Depending on **bit 1** of the **APC signals register**, the chip now operates in either of two modes:

- If **bit 0** is set to **0**, the chip operates in **sample (S) mode**.
- If **bit 1** is set to **1**, the chip operates in **readout (R) mode**.

The Sample Mode

In sample mode (OUT/$\overline{\text{SR}}$ = 1, APC signals register bit 1 = 0), the signals CLK1, CLK2 and BIN are transferred to the outputs SPHI1, SPHI2, and SBI, respectively. The complementary outputs RPHI1, RPHI2, and RBI are set to 0.

Additionally, the signals SPHI1, SPHI2 are used internally to clock a further 32–bit shift register, which takes the SBI signal as input.

This shift register therefore runs synchronously with the corresponding shift register on the APC128 chip.

In normal operation, SBI is set to 1 for one clock cycle and then to 0 during the next 31 clock cycles; this single bit is then shifted through a 32–bit shift register, which determines the pipeline stage into which is written on the APC.

On the decoder chip, this bit is likewise shifted through a 32–bit shift register. This bit then determines which bit from the **calibrate register** is sent to the **calibrate output**.

The Readout Mode

In readout mode (OUT/$\overline{\text{SR}}$ = 1, APC signals register bit 1 = 1), the signals CLK1 and CLK2 are transferred to the outputs RPHI1 and RPHI2, respectively.

The signal BIN is also transferred to the output RBI, provided the input signal RBE (Read Bit Enable) is set to 0[1], otherwise it is kept in its previous state.

The complementary outputs SPHI1, SPHI2, and SBI are set to 0.

The APC Signal Register

As already discussed, the APC signal register is filled in shift register mode, and its first four bits are used during output mode to set either sampling or readout mode (bit 1), and to decide whether the contents of the calibrate, control, and current supply registers are updated from the shift register contents.

The remaining 12 outputs of the APC signals register go to output pins, and have in the context of the H1 CST the following meanings:

Bit	Signal
5	Reset
6	IS
7	SR
8	R12
9	CS
10	SEB
11	LE

Bits 12 to 16 are also connected to pins.

In the context of the H1 CST readout always two neighboring ladders are read out together, first one (“early” ladder), then the other (“late” ladder). To

[1] Check this!

synchronize this, for early ladders bit 12 is connected to the RBE input, for late ladders bit 15 is connected to RBE.

Note that all the outputs of the APC signals register are **inverted** with respect to the input bits! Therefore, to set e. g. the CS output to 1, a 0 must be fed into bit 9 of the shift register!

The Calibrate Register

As already discussed, the calibrate register is a 32–bit register that is filled from the shift register if bit 2 of the APC signals register is set to 0.

In the calibrate register an arbitrary 32–bit pattern can be stored.

In output mode, more precisely, in sampling mode, usually a single 1–bit (coming from the BIN inpout) is clocked through a 32–bit shift register. The 32 outputs of this register steer transmission gates which each connect one output of the calibrate register with the calibrate output.

Therefore, if a single bit is clocked through the shift register every 32 clock cycles, the contents of the calibrate register are sequentially put onto the calibrate output.

This feature can be used for test purposes.

The Control Register

As already discussed, the calibrate register is a 8–bit register that is filled from the shift register if bit 3 of the APC signals register is set to 0.

This register operates an array of 8 switches, which are each connected to one pin (SW1 to SW8) on one side and to a common pin (SW) on the other side.

The switch corresponding to a certain bit is **closed** if the bit is set to **0**, and open if it is set to 1.

Therefore, after a fast reset all switches are closed!

In the context of the H1 CST, this register is used to connect various signals (reference and other voltages) to the SW output. In this application care has to be taken that at most one swich is closed at any time, because otherwise two voltages are connected which may destroy the switch array.

The Current Supply Register

As already discussed, the calibrate register is a 8–bit register that is filled from the shift register if bit 4 of the APC signals register is set to 0.

The first seven bits of this register are used to steer a digital–analog converter (DAC) on the decoder chip, which acts as a current source.

The DAC consists of a set of FETs, which have different dimensions such that each bit corresponds to a different current that is let through by the transistor. A transistor is **conducting** if its corresponding bit is set to **1**.

Note: The smalles transistor is connected to bit 1, and the most powerful transistor to bit 7. This must be kept in mind when the `h1cpg` programis used to generate the sequencer pattern.

Therefore, to set the smallest current different from 0, use the following sequence:

```
SR
MOV8 ???0 ????  ????  ????  x?????????  x??  10000000
OUT
```

To get the maximum current, use the following sequence:

```
SR
MOV8 ???0 ????  ????  ????  x?????????  x??  11111110
OUT
```

At the H1 CST, this feature is used to define the operating current of the APC chips.

The eighth bit of the current supply register is put to a special pin, called RG.

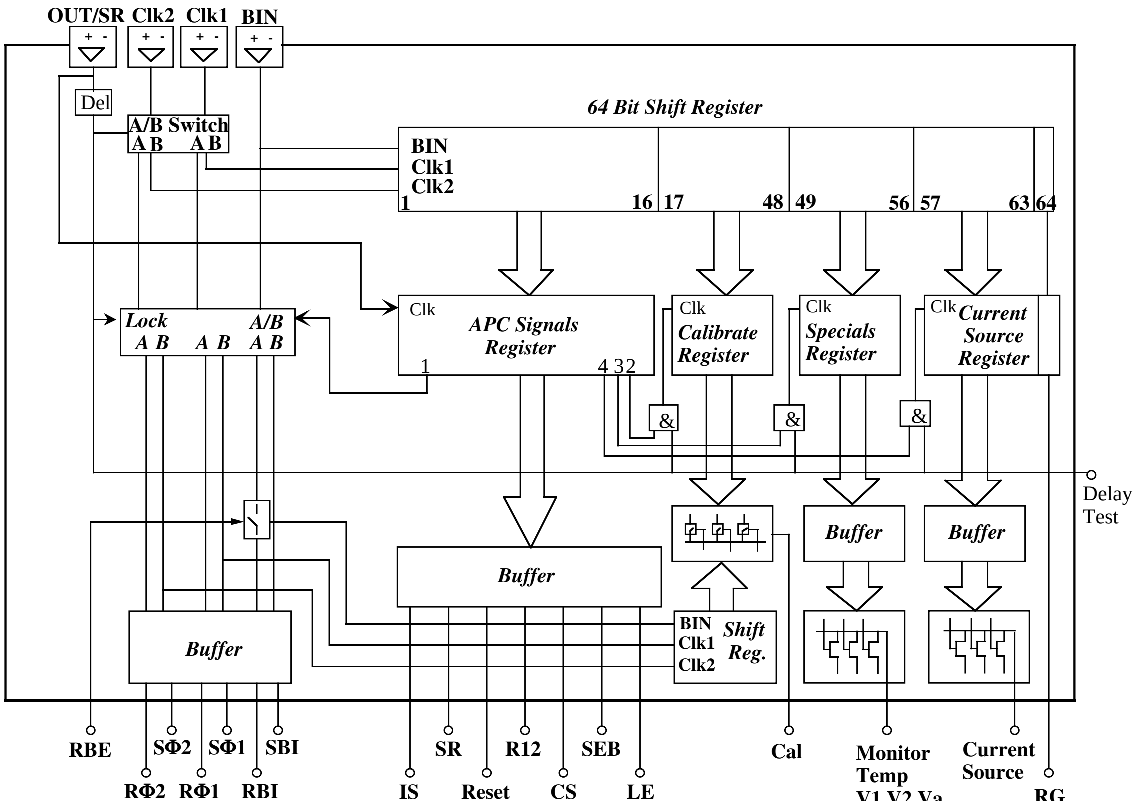

Figure 5: Schematic view of the H1 decoder chip.