Testing the H1 CST Decoder Chip

Benno List

ETH Zürich, IPP

29.5.2000, 9.3.2001

Reset Test

Program: `test1.src`

What is tested: How much time is needed to fast clear the whole shift register.

Signals to look at: OUT8 (last bit of the current supply register)

What to do: Run the program and vary the clock speed of the pattern generator until OUT8 does not go to 0 any more. The time of one external clock cycle is then the minimum time for a fast reset.

How it works: After an initial reset, the program goes into a loop. In this loop, the shift register is first filled with ones (only bits 1–4 are set to 0). After that, a fast reset is done. If the fast reset signal is too short, the last bit of the shift register will not go to 0 anymore.

Output ModeTest

Program: `test2.src`

What is tested: Switching between sample and output mode

Signals to look at: SPHI1, SPHI2, SBI, RPHI1, SPHI2, RBI, compare to CLK1, CLK2, BIN

What to do:

- Check the relative timing between SPHI1/RPHI1 and CLK1, SPHI2/SPHI2 and CLK2, SBI/RBI and BIN.
- RBI should show a sequence $0 - 1 - 00 - 1 - 0 - 1 - 000$ every second time when OUT/$\overline{\text{SR}}$ is 1.
- SBI should show a sequence $0 - 1 - 0 - 11 - 0 - 111 - 0$ every second time when OUT/$\overline{\text{SR}}$ is 1.
- Check the function of the RBE signal.

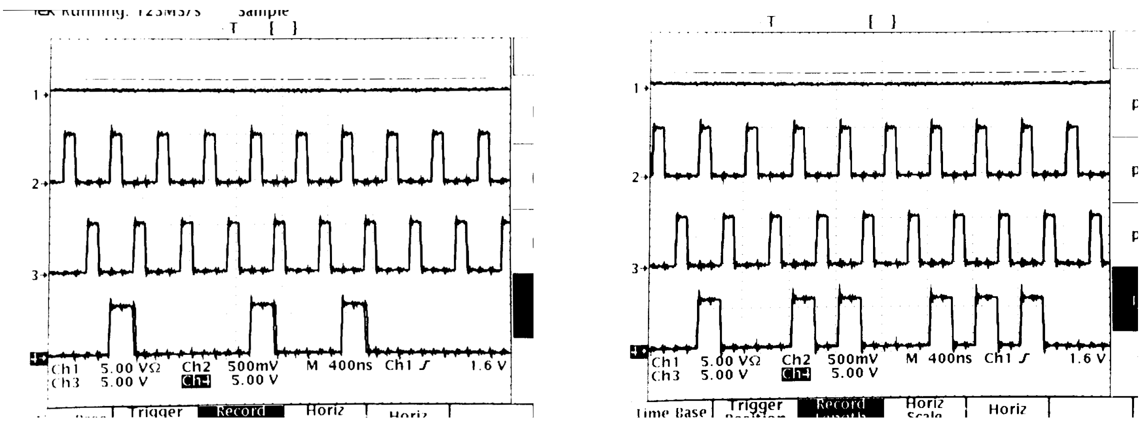

Figure 1: Scope view of the $R\Phi1$, $R\Phi2$, and RBI signals (left) and the $S\Phi1$, $S\Phi2$, and SBI signals (right) for TEST2.

APC Signals Register TES

Program: `test3.src`

What is tested: The signals from the APC signals register.

Signals to look at: SBI, RESET, IS, SR, R12, CS, SEB, LE, SIGNAL12, SIGNAL13, SIGNAL14, SIGNAL15, SIGNAL16

What to do: Look on SBI, two zeroes indicate the start of the pattern. Look at the other signals in turn signals and identify them by their bit patterns:

Pin	Bit	Name	Pattern
14	5	Reset	111111 – 000
15	6	IS	1111 – 0 – 1 – 000
16	7	SR	111 – 0 – 11 – 000
18	8	R12	111 – 00 – 1 – 000
19	9	CS	11 – 0 – 111 – 000
29	10	SEB	11 – 0 – 1 – 0 – 1 – 000
13	11	LE	11 – 00 – 11 – 000
63	12	SIGNAL12	11 – 000 – 1 – 000
57	13	SIGNAL13	1 – 0 – 1111 – 000
58	14	SIGNAL14	1 – 0 – 11 – 0 – 1 – 000
59	15	SIGNAL15	1 – 0 – 1 – 0 – 11 – 000
62	16	SIGNAL16	1 – 0 – 1 – 00 – 1 – 000

Calibrate Register Test

Program: `test4.src`

What is tested: The calibrate register

Signals to look at: SBI, Calibrate

What to do: Observe the Calibrate output. It should show a pattern 0-1-00-1-000-1-0000-1-00000-1-000000-1-0000-1

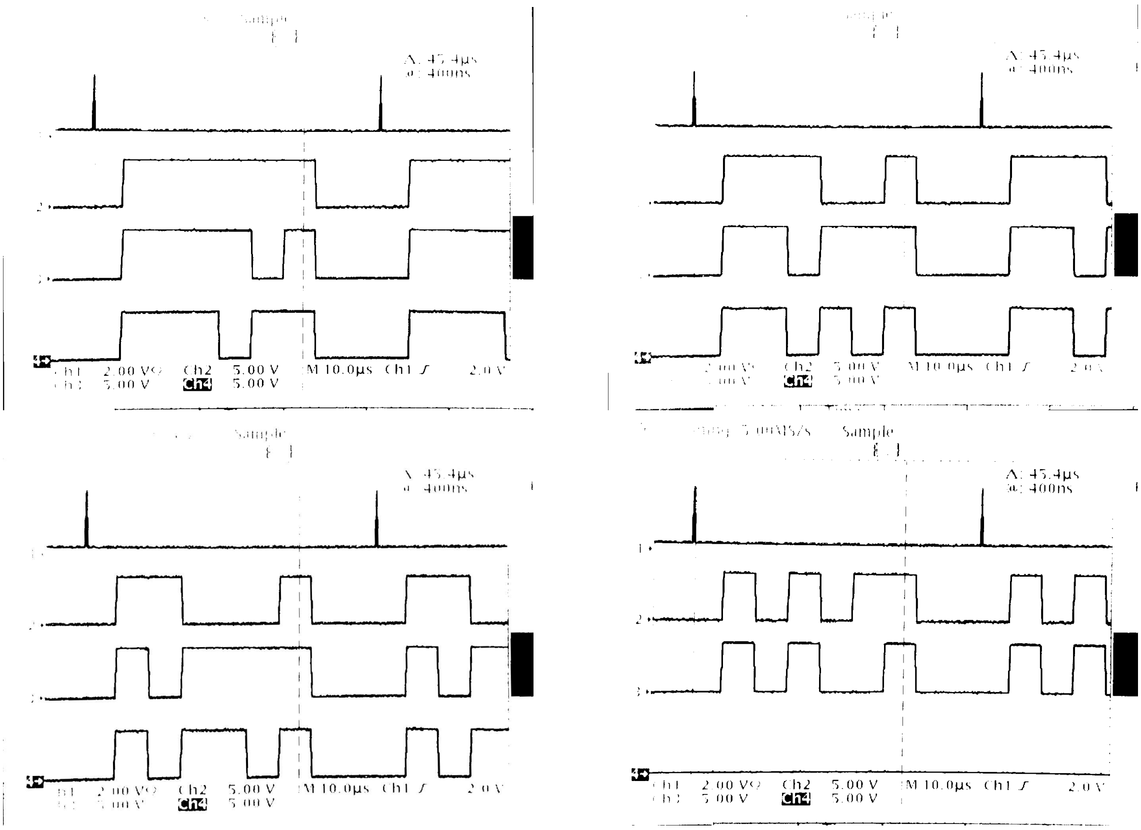

Figure 2: Scope view of the signals for TEST3:
upper left: Reset, IS, SR; upper right: R12, CS, SEB
lower left: LE, Signal12, Signal13; lower right: Signal15, Signal16

Control Register Test

Program: `test5a.src`

What is tested: The control register

Signals to look at: SBI, SW

What to do: Connect a series of resistors to SW1 to SW8 such that the voltage on SW1 is $V_{DD}/8$, on SW2 is $2V_{DD}/8$, and so on up to SW8 with V_{DD}. Look at SW. It should show a staircase pattern.

Current Supply Register Test

Program: `test6.src`

What is tested: the current supply register

Signals to look at: The current source output and DAC8

What to do: Connect a voltage to V_{DAC}. Monitor the current source output. It should show a staircase pattern with the following values: 0, 1, 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 112, 120, 124, 126, 127, 0. At the end of the

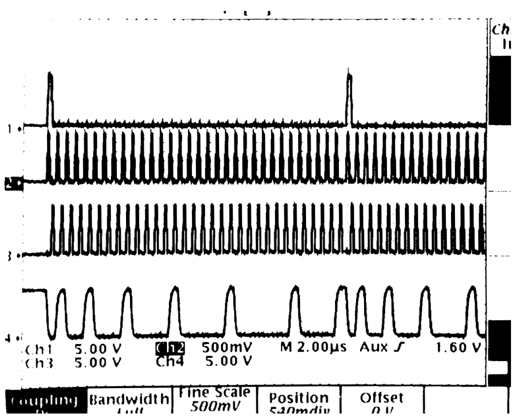

Figure 3: Scope view of the $S\Phi1$, $S\Phi2$, SBI, and CAL signals for TEST4.

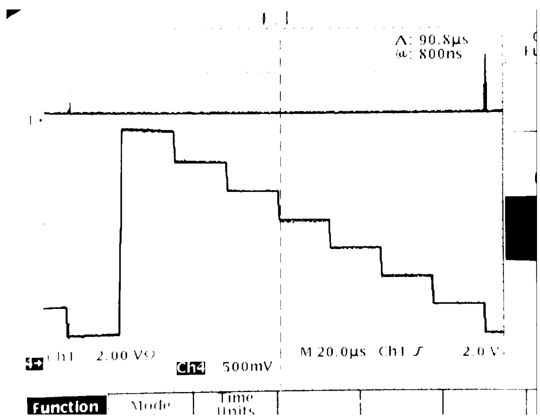

Figure 4: Scope view of the SW signal for TEST5A.

staircase, OUT8 should show a "1".

Latch Function Test

Program: `test7.src`

What is tested: The latch functionality of the APC signals register.
Signals to look at: Calibrate, SW, Current source, DAC8
What to do:

- Check the calibrate signal. It must stay at 0.
- Connect a resistor chain to SW1...SW8. Check SW. It must not show any activity.
- Connect a voltage to V_{DAC}. Observe the current source and DAC8. No changes must be visible.

How it works: The program loop clears the shift register and transfers its contents to the APC signals register, the calibrate register, the control register, and the current supply register. Then it sets the shift register to various bit patterns which should not be transferred to the buffers.

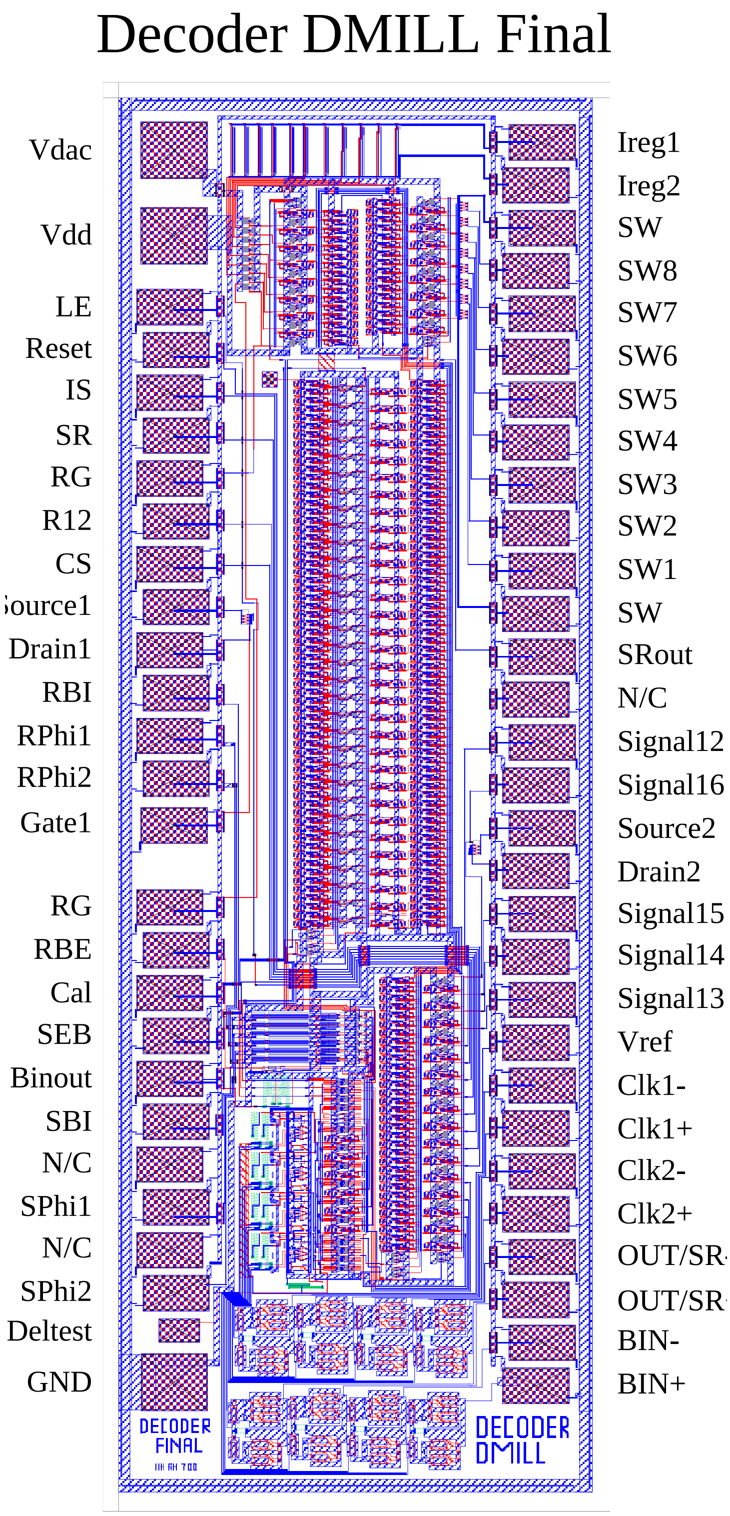

Figure 5: Layout of the DMILL decoder.

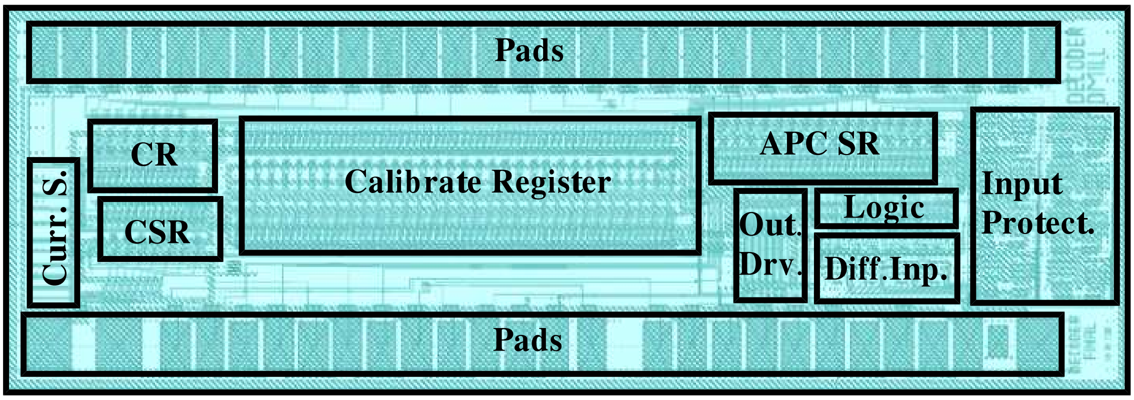

Figure 6: Overview over the decoder chip.
The abbrevations stand for: **Curr. S.**: current source, **CR**: control register, **CSR**: current supply register, **APC SR**: APC shift register, **Diff Inp.**: differential inputs, **Out Drv**: output drivers, **Input Protect.**: input protection.

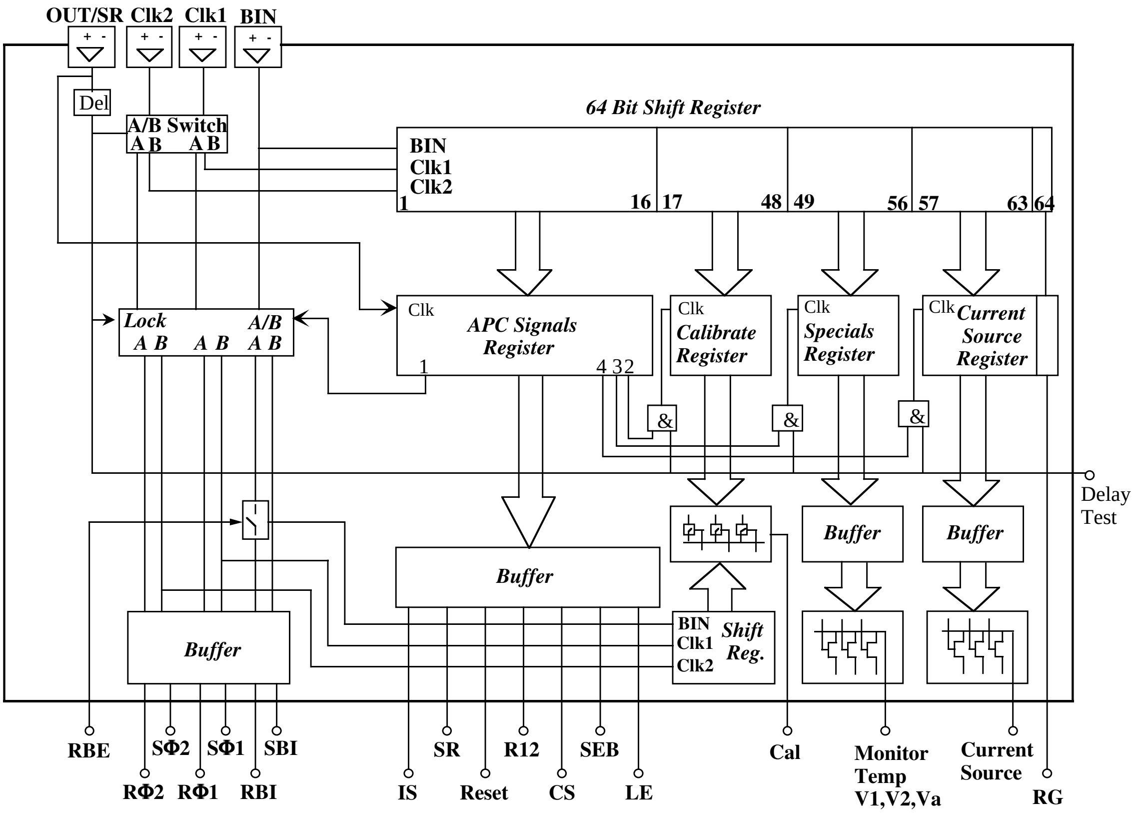

Figure 7: Schematic of decoder.

Bondplan Decoder DMILL
auf Chipcarrier

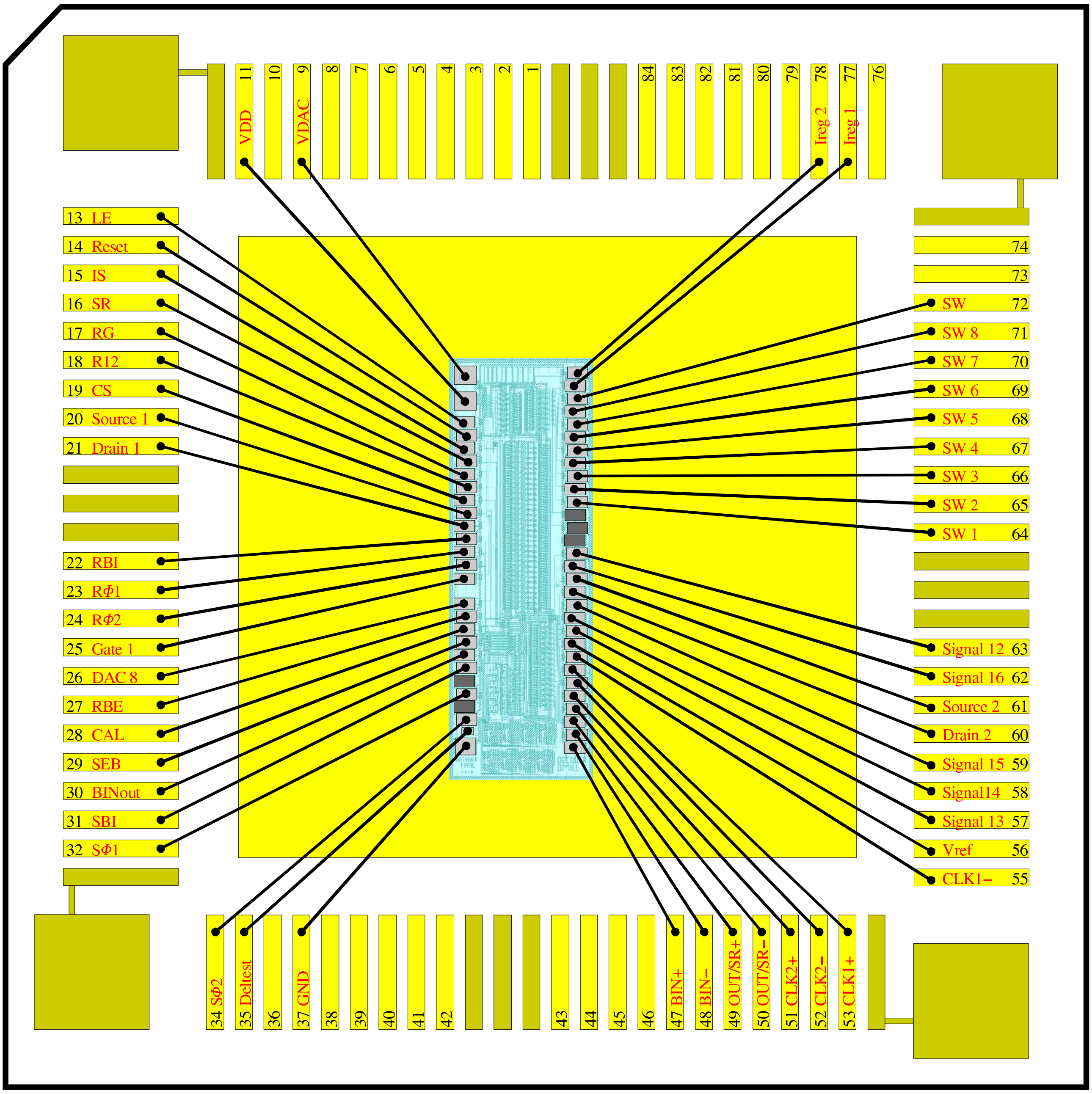

Figure 8: Bonding scheme for the decoder on the test chip carrier.

B. List 4.4.00, 8.3.01

/home/blist/cst/chips/decoderfinal−bondplan−test.sdc