Optical Analog Readout and Control of the Central Silicon Vertex Detector of H1 at HERA

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Abstract

The fast and slow control of the Central Silicon Tracker in H1 is performed by means of an ASIC decoder chip having four digital input lines. These control signals as well as the analog hit signals are transmitted to and from the detector through 34 m of optical fibers, which are composed of three connectable multifiber cables.

1 Introduction

Silicon vertex detectors have become standard equipment of large collider experiments[1, 2, 3, 4, 5, 6]. They provide position resolutions of around 15 μm at the expense of a large number of readout channels concentrated in a small volume. This requires VLSI frontend electronics which have the task of signal amplification and of keeping the data until a trigger decision initiates multiplexed readout. Up to now the time between bunch crossings exceeded the trigger decision time (e.g. at LEP, SLC and Tevatron), allowing the readout of a triggered event to be finished before the following bunch crossing would occur.

At HERA the time between collisions is only 96 ns and the data of typically the last 25 bunch crossings have to be stored in a data-pipeline at the frontend to await a trigger decision. A chip incorporating 128 channels of preamplifiers and 32 buffer deep analog pipelines (APC128)[7] has therefore been developed for the Central Silicon Tracker (CST) of H1[8].

In this paper we describe the control of the APC128 via digital signals transmitted through optical fibers, and the optical transmission of the analog data. Optical communication has the advantage of immunity against electromagnetic interference and moreover of less material in front of other detectors ($X_0(glass)/X_o(Cu) = 8.8$). A suitable fiber diameter and signal transmission speed allows for a solution with low power consumption at the frontend. The design includes the transmission of some slow control values (voltages, temperatures), and monitoring the transmission of the 34 m long optical lines which are composed of three cables coupled together with two optical connections.

Optical data transmission is already in use for the L3 microvertex detector [6], where the signals are digitised near the frontend and the zero-suppressed digital data is transferred via optical fibers[9]. This requires cooling of the FADC units inside the detector. Optical analog data transmission has also been used before [10].

2 System Layout

The central silicon tracker of H1 consists of two coaxial layers of 12 and 20 silicon ladders with an active length of 35.8 cm. The first half shell has been installed in H1 for the 1995 running period (figure 1). The sensors [11] are double sided, with 640 DC-coupled readout lines on each side. Hybrids made from $A\ell N$ carry on both faces five APC128 chips and the pertinent control circuit with an ASIC *Decoder Chip* as the center piece (figure 2). Figure 3 shows the electrical and optical system layout. Signals from the silicon sensors are amplified and stored in the switched capacitor pipeline of the APC128 chip, see figure 4) [7]. The pipeline is continuously operated with the HERA clock of 10.4 MHz until a trigger signal arrives and stops it. During the subsequent readout the pipeline buffer of the corresponding time slice of each channel is connected sequentially to the output amplifier, brought via a 5 cm long flat and flexible Kapton cable to a printed circuit at the end of the detector and converted into optical signals. Two p-sides (n-sides) of two adjacent half-ladders are daisy-chained and connected to a single fiber which transmits 1280 channels per event. The reconverted signals are digitised in the *Online Silicon Readout Controler* (OnSiRoc) [12].

The control signals for the APC128 are generated in the decoder chip. For each mode of operation of the APC128 a specific bit sequence is loaded into the 64 bit decoder chip shift register (figure 5). This bitstream is prepared in a sequencer in the (OnSiRoC) [12] located outside the experiment some 34 m away. Since all APC128 chips need at any given time the same control sequence, all decoder registers can be loaded simultaneously via four optical lines.

3 Decoder Chip

The decoder chip (1.2×2.4 mm^2) is built in SACMOS 1 technology (1.2μm feature size) [13]. It is placed on each face of the hybrid and generates various control bit patterns applied to the APC128 chip. In addition it performs some slow control functions and allows calibrations. Bit patterns can be loaded sequentially into a 64 bit shift register through one data line and using two clocks and one control line (see figure 5). The first four bits serve for internal control of the chip. Bits 5 through 11 generate seven signal levels applied to the APC128. The next five bits are available for other purposes. 32 lines are reserved for the *Calibrate Register*, eight bits for the *Slow Control Register* and seven signals for the *Current Supply Register*. The last bit allows, if connected, to choose a feedback resistor value of the APC128 preamplifiers, that is either lower (bit low) or higher (bit high) than the default resistor value.

The electronics for the n-side of the DC-coupled sensors has to operate at the bias voltage. The four input lines for the decoder have therefore to be AC-coupled. In our solution the input comparators on the decoder chip (figure 6) have two stable states and switch from a high output state to a low output state and vice versa with an input signal difference of 600 mV through coupling capacities of only 15 pF. For system uniformity the inputs to the decoder chip for the p-sides are also AC-coupled.

3.1 The Pipeline Control via the Decoder Chip

The decoder chip runs in two main modes of operation which are selected with the switch OUT/SR (see figure 5). In the mode OUT the input signals BIN (bit-in), Clk1 (clock1) and

Clk2 (clock2) are, depending on the value of bit 1 of the shift register, directly connected to the outputs $S\phi1$ or $R\phi1$, $S\phi2$ or $R\phi2$, and SBI or RBI, corresponding to the *Sampling Phase* (operating the pipeline shift register of the APC128), or the *Readout Phase*. The second mode SR is the downloading of the 64 bit shift register of the decoder. In this case the switch OUT/SR is in the position SR (*S*hift *R*egister) and the signal BIN is shifted into the register using the clocks Clk1 and Clk2. The cycle frequency is kept at 10 MHz for sampling and downloading, and 2 MHz for readout, respectively.

The decoder also allows routing of the readbit-in (RBI) signal. In our case the input RBE (readbit enable) is hard-wired to either one of two available bits and operates a switch which enables or inhibits the RBI signal. In this way two p-sides (n-sides) can be read out successively through the same readout channel.

3.2 Calibration and Slow Control via the Decoder Chip

An important part of our detector with no access during most of the year is a sophisticated monitoring and calibration system. These control tasks are also performed by the decoder chip.

Calibration signals can be distributed to each preamplifier input of the APC128 by means of a shift register on the decoder chip running synchronously with the *Pipeline Shift Register* on the APC128, and the 32 bit *Calibrate Register* which determines which of the 32 pipeline buffers will be filled with the calibration pulse.

The decoder chip is equipped with a DAC that is connected to the seven bit *Current Supply Register*. The output of the DAC drives a current source on the hybrid (*pnp*-transistor SA MMBTA56) for the preamplifiers on the APC128 chip.

For calibration of the analog readout chain and other control functions, the LED driver can be supplied sequentially with a set of voltages (see figure 3) denoted by *Temp.Control,* V_1, V_2 and V_a in figure 5. The voltages V_1 and V_2 are derived from a reference voltage obtained from an AD580 chip on the hybrid, and serve for calibration of the transmission line. V_a is the voltage for the APC128 preamplifiers as generated by the current source. A drift of V_a at fixed current can be caused by radiation-induced threshold voltage shifts in the CMOS transistors. By repeated reloading of the 8 bit *Slow Control Register*, V_1, V_2, V_a and an NTC resistor for temperature measurement are connected to the output stream, and the data appended to each event.

4 Electrical-Optical Converter

The design criteria for the optical transmission system was low heat dissipation, minimum geometrical dimensions and immunity against radiation damage at the 100 krad level. Rise times of $\leq$ 5 ns for the digital control signals are required. Figure 7 presents our solution for the optical signal drivers. We use LED diodes with pigtails (see section 5), and a very simple amplifier for the analog driver. This amplifier together with the LED has a linearity of better than 1% for a current range $i_{LED} \, \epsilon \, [8, 16]$ mA and a temperature stability of 10% gain change for a temperature variation $T \, \epsilon \, [20, 50]^oC$. Gain variations of the BFR93 transistor are compensated by selecting R_E in fig. 7. The parasitic input capacity of the circuit is only 2.3 pF, which is small compared to the capacity of the signal line on the hybrid from the APC128 to the LED driver. This latter capacity limits the rise time of the analog pulse to about 200 ns and determines the maximum readout speed of the APC to about 2 MHz.

The optical receivers for analog and digital signals are displayed in figure 8. The bandwidth of the analog receiver is limited to 20 MHz to minimize noise. We measured the noise of the whole readout chain

$$i^2_{noise}\ [nA^2] = (21)^2 + 13.2 \cdot i_{PIN}\ [\mu A]$$

where the PIN-diode current in the receiver is of order 10μA. This corresponds to a noise:signal ratio for a minimum ionising particle through the silicon sensor of 0.01. The noise voltage distribution has a purely Gaussian shape over a wide range as depicted in figure 9, which demonstrates the immunity of the optical signal transfer against pick-up noise.

Table 1: Power consumption of various components used in the readout chain at the detector site.

device	power per strip	power for full detector
APC128 preamplifier	0.23 mW	18.8 W
current source	0.06 mW	4.9 W
Decoder and APC128 digital part	0.20 mW	16.4 W
LED driver	0.04 mW	3.2 W
PIN diode receiver	0.05 mW	4.0 W
total power	0.58 mW	47.3 W

The total power consumption at the detector is summarised in table 1. The power of all components is given both per silicon strip and for the full detector. Note that the LED driver is only active during data readout and idle during pipeline operation, and uses therefore less power during the latter. About 1.5 m away from the detector there are voltage regulators consuming 8 W.

The behaviour of the optical drivers/receivers has been tested after radiation damage applied with a Co^{60} source. For a dose of 100 krad the gain has changed by 3%. It can be recalibrated on-line whenever necessary.

5 Optical Fibers and Connectors

The optical lines are 34 m long and must have two breakable connections for insertion reasons. In telecommunication, where signals have to travel over large distances, monomode fibers with a core diameter of 7 μm are used. In a typical particle physics experiment the distances are of order 10-50 m, and multimode fibers with a transmission bandwidth of 20 MHz·km are sufficient. Such cables can have core diameters of a few 100 μm. Large fiber diameters are preferable for efficiently coupling the light of the LED diodes into the fibers, and for being insensitive to small misalignments at the connections, offering cheaper solutions. Mechanical stress when bending a multifiber bundle on the other hand is less for small diameter fibers, so we selected as a compromise a fiber core diameter of 200 μm (230 μm cladding diameter, total fiber diameter 500 μm). A halogen-free cable with nine fibers has been manufactured by Huber and Suhner [15].

A miniature 9-fold optical multiconnector (3×3 matrix) has been designed (see Figure 10). For assembly, the coating at the fiber end is removed, the fiber is inserted from behind into the connector body (Aluminium) and glued with Araldit S50 [16]. The fiber tips exceeding the front face of the connector are cut and glued with Epo-tek 302 [17]. Then the connector face is polished.

Light losses have been measured to be around 40% through two naked connections and 15% when optical grease is used. These numbers are reproducible for repeated connections within 10%. The connector has been patented in Switzerland [14].

At the fiber ends, diodes are attached which are plugged into transistor sockets. For assembly of these pigtails, the diodes are provided with housings as shown on the left side of figure 11. The fiber ends are glued into small tubes (see right side of figure 11) as described above for the multifiber connector. The tubes with polished faces are then glued into the diode housings. The relative orientation of the two parts is optimized for maximum light transmission.

Acknowledgement

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[16] Ciba Geigy, CH 4000 Basel, Switzerland.

[17] Polyscience AG, Riedstr. 13, CH 6330 Cham, Switzerland.

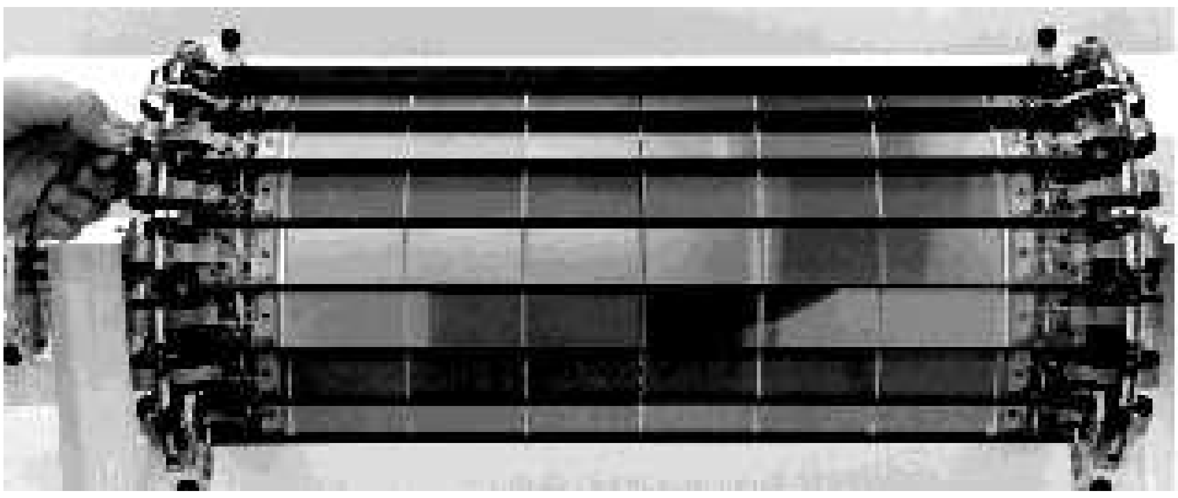

Figure 1: Half shell of the Central Silicon Tracker of H1.

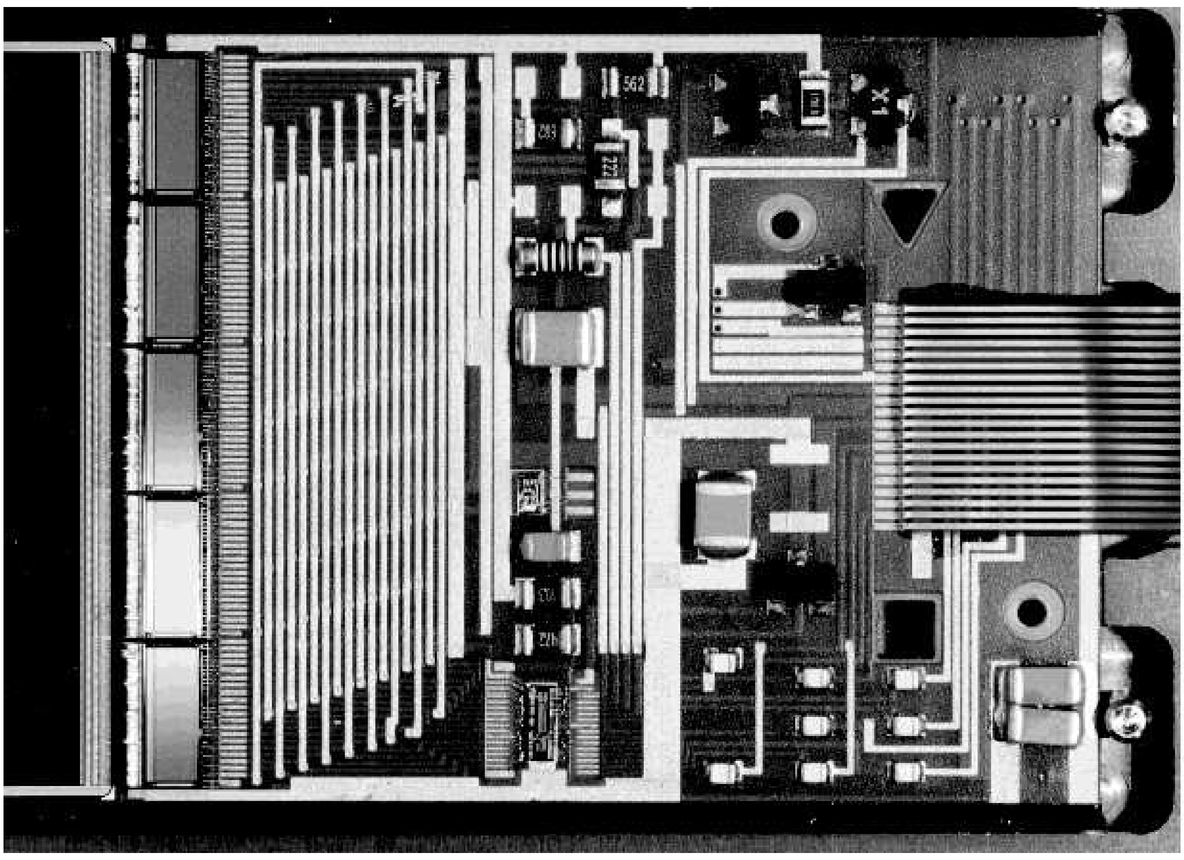

Figure 2: p-side of the hybrid made from 635 μm $A\ell N$. Left: Five preamplifier chips (APC128). Low center: Decoder Chip.

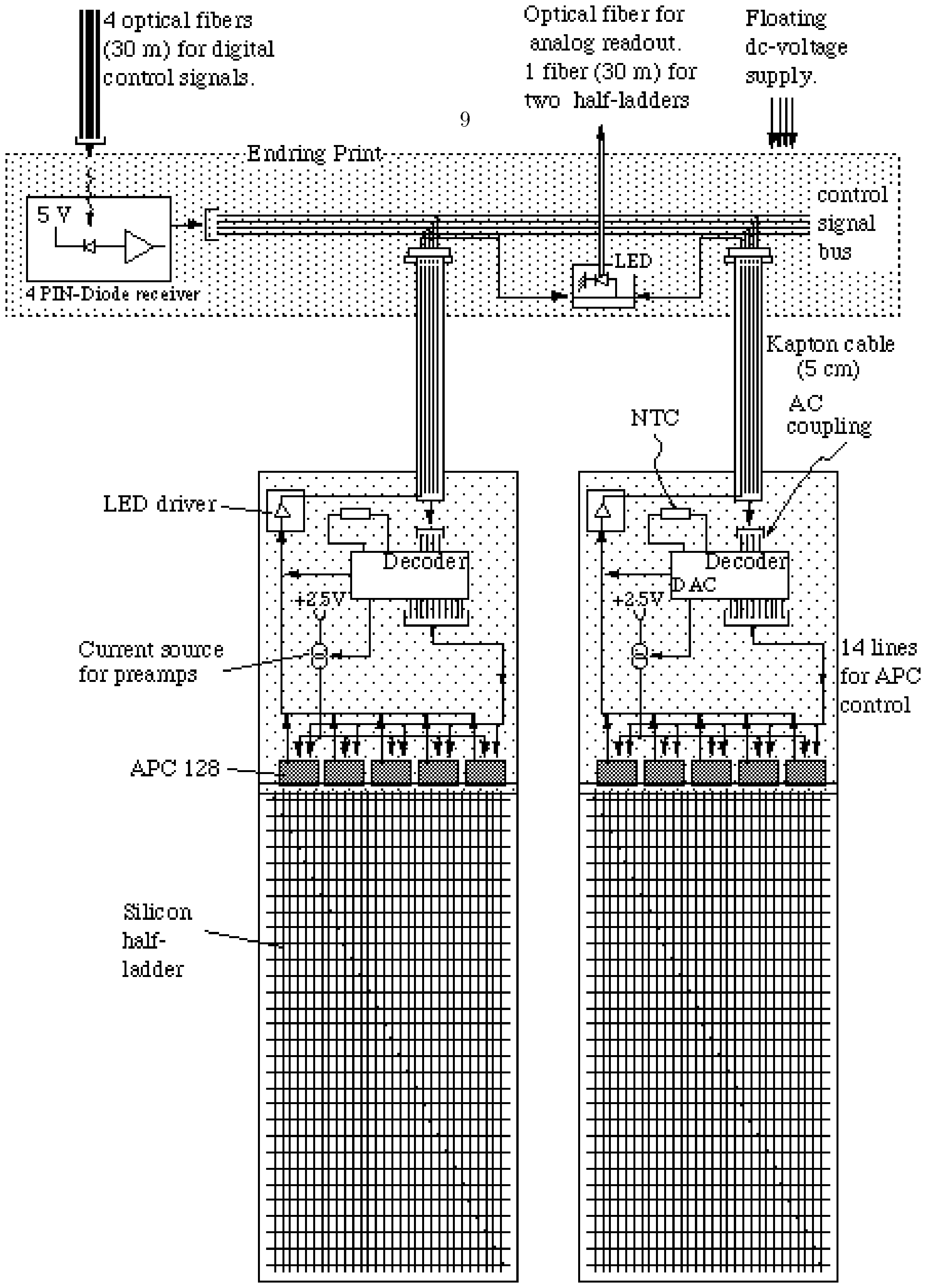

Figure 3: Schematic layout of the electrical and optical readout and control.

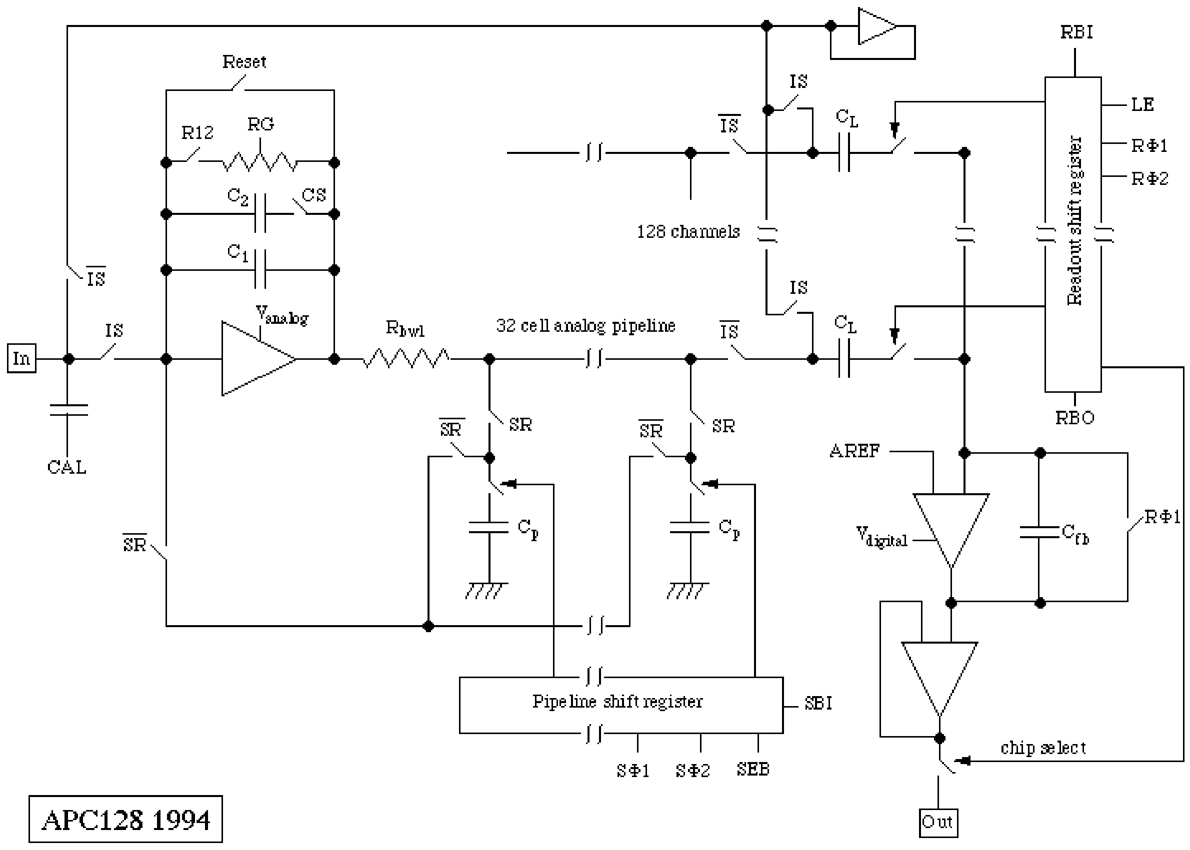

Figure 4: Simplified diagram of APC128 chip.

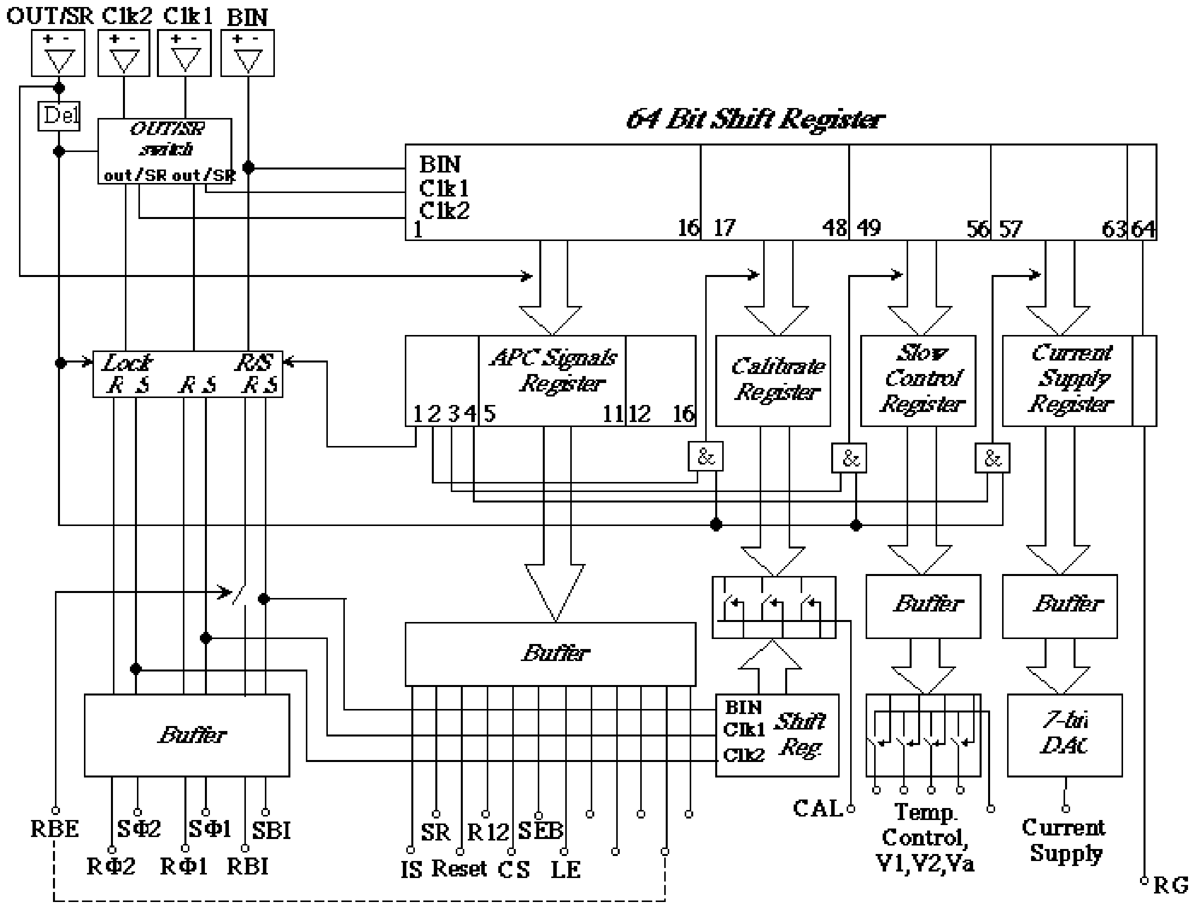

Figure 5: Layout of Decoder Chip.

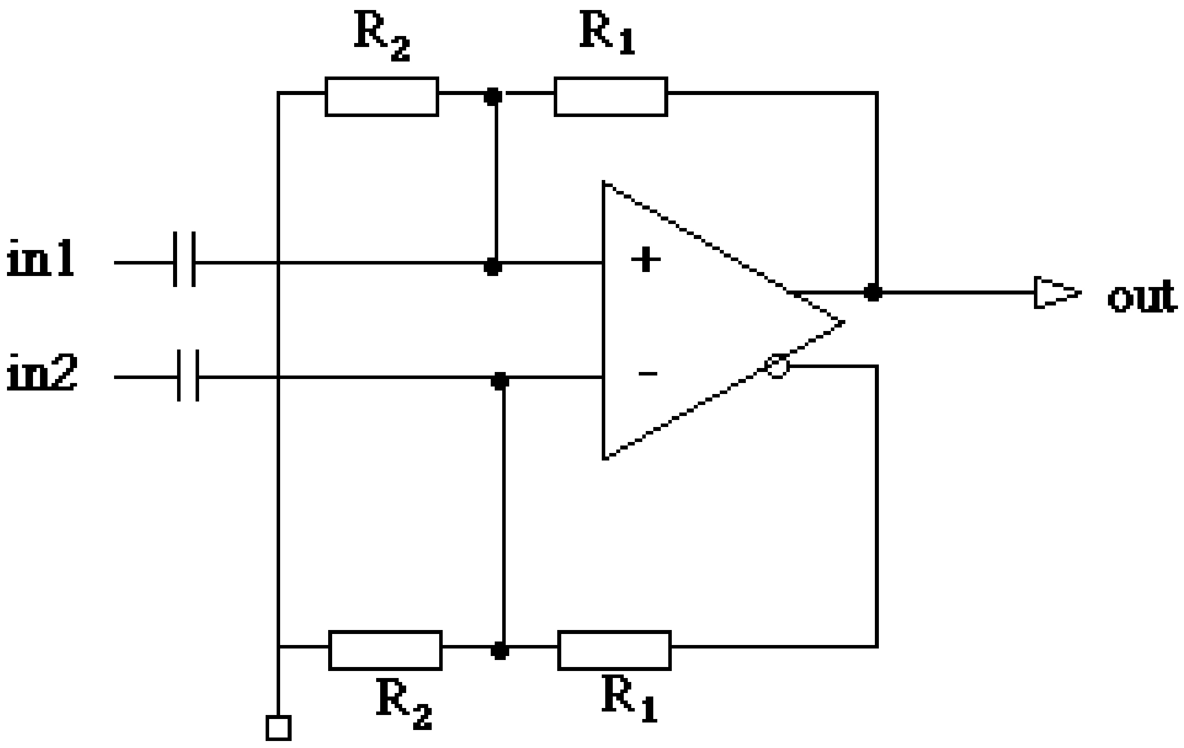

Figure 6: Circuit diagram of the input stages of the decoder chip. The capacitors are external to the decoder chip.

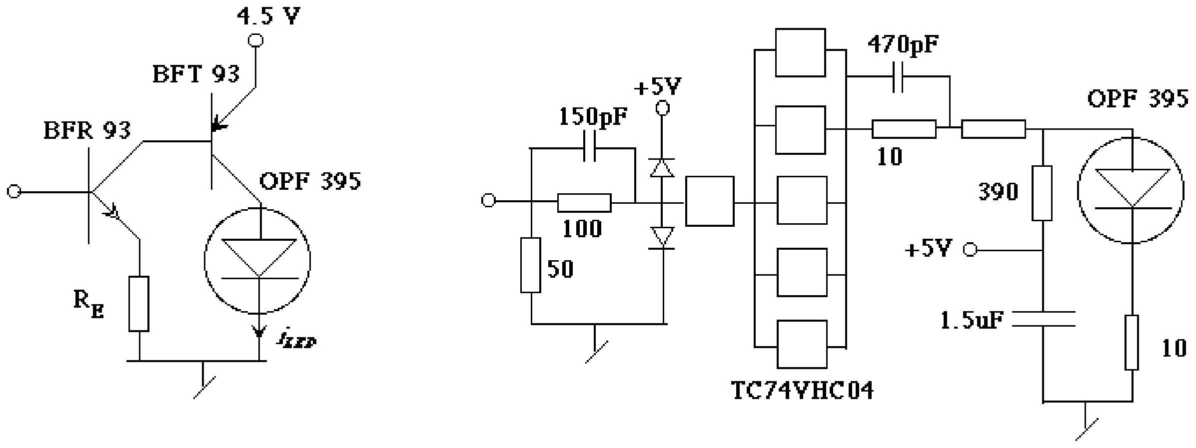

Figure 7: Circuit diagram of the electrical-optical converters. Left: Analog signal driver situated on the hybrid (with the exception of the LED). Power consumption 50 mW. Right: Digital signal driver situated 34 m apart from the detector.

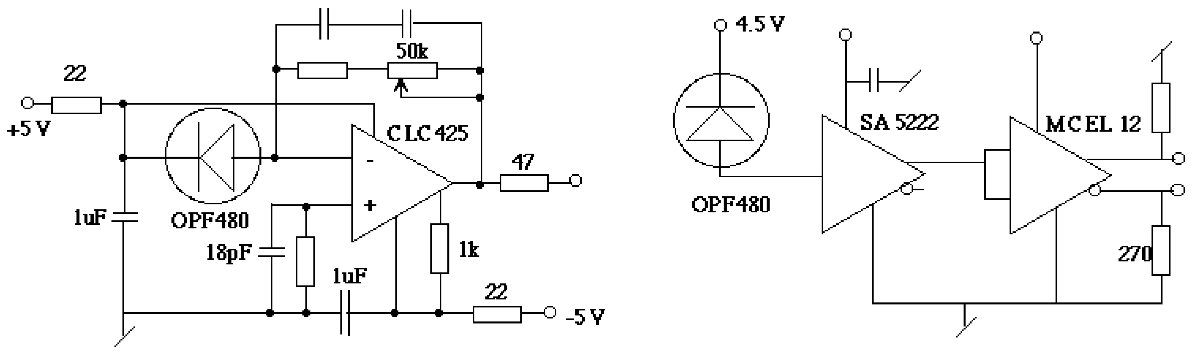

Figure 8: Circuit diagram of the optical-electrical converters. Left: Analog signal receiver situated 34 m apart from the detector. Right: Digital signal receiver situated on a printed circuit at the end of the detector. Power consumption 250 mW.

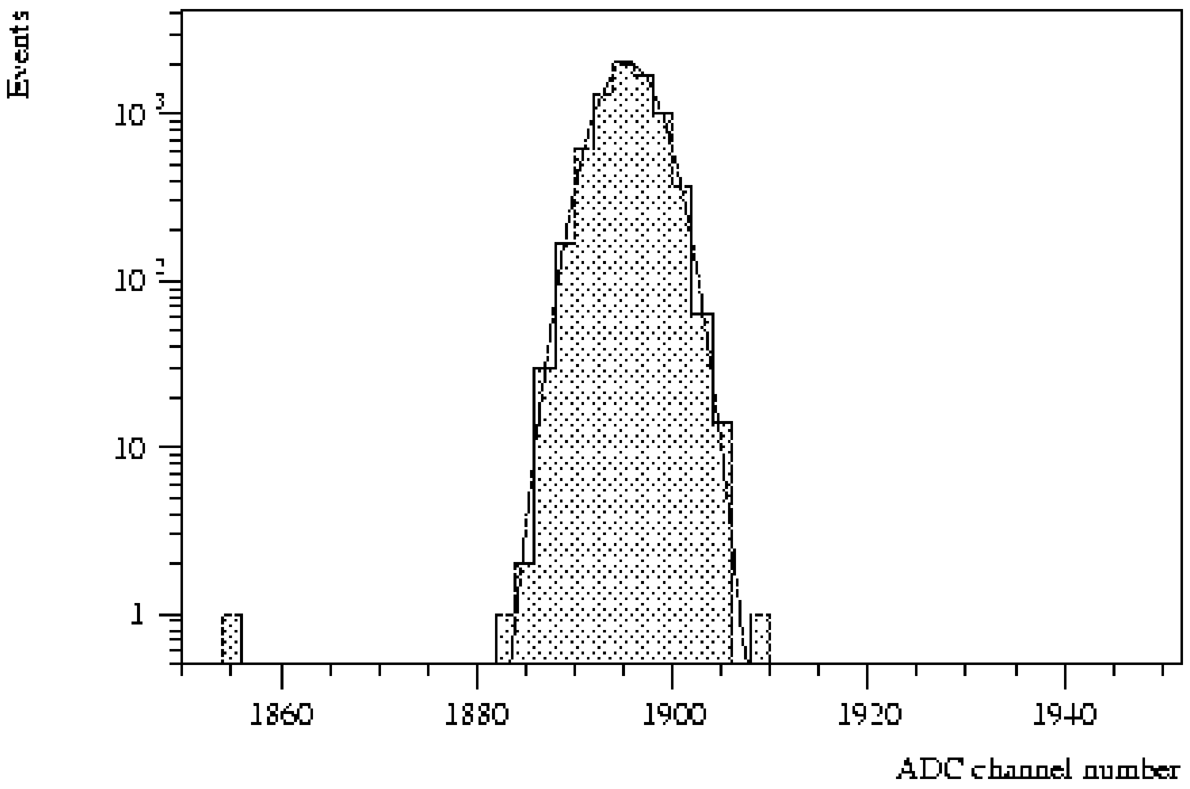

Figure 9: Distribution of measurements of a reference voltage (2V) transmitted through the optical readout chain and digitised with a 12 bit FADC. The distribution is purely Gaussian with an r.m.s of 2.9 bits. For comparison: Signals from the APC128 have a noise contribution of 32 bits.

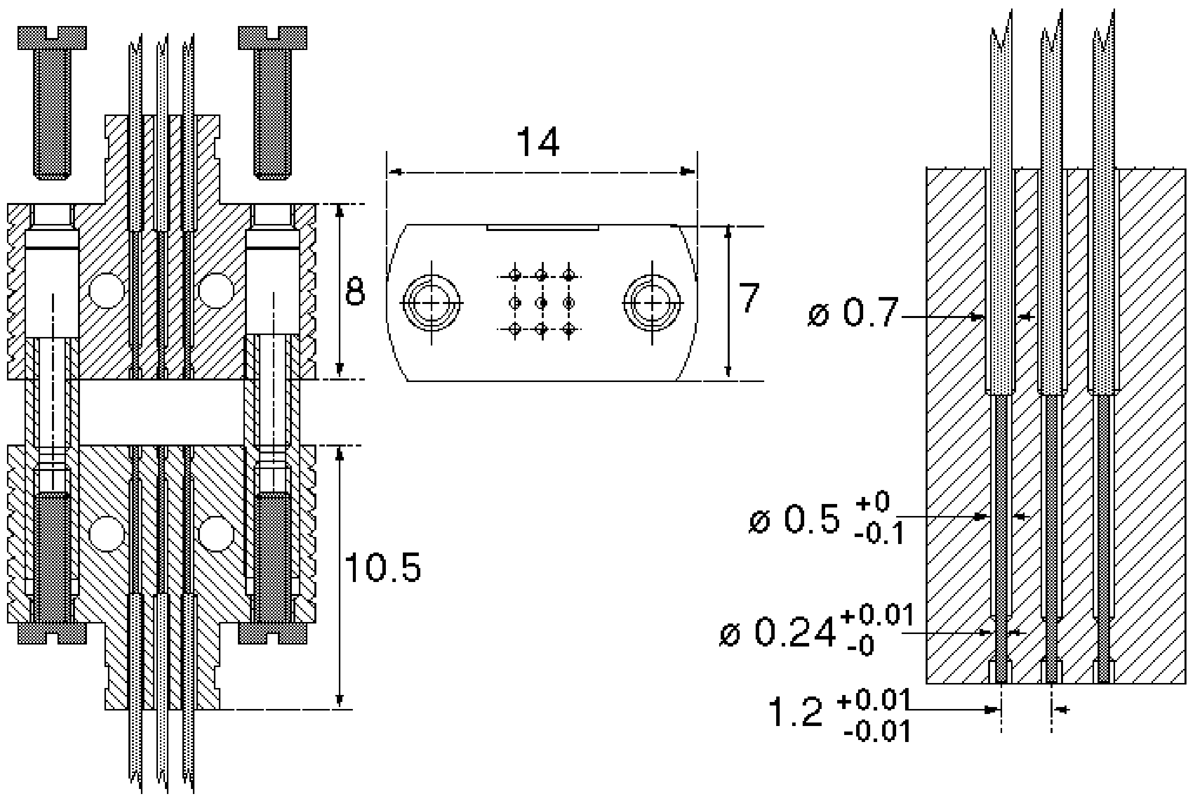

Figure 10: Pair of optical multiconnectors (left) and enlarged view of the central part with fibers glued in (right).

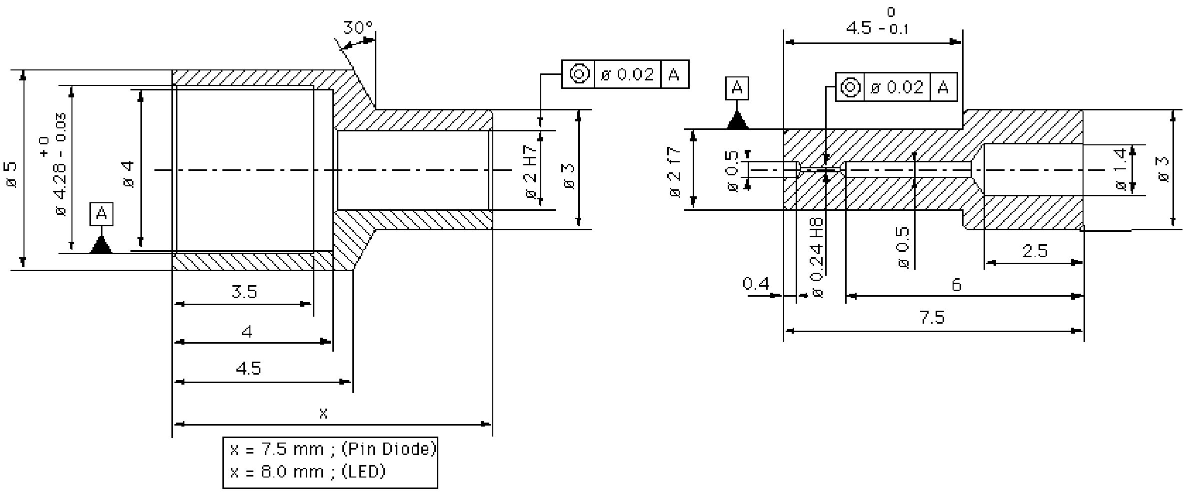

Figure 11: Left: Housing for diode. Right: fiber end.