The H1 Central Silicon Tracker: Performance and Upgrade

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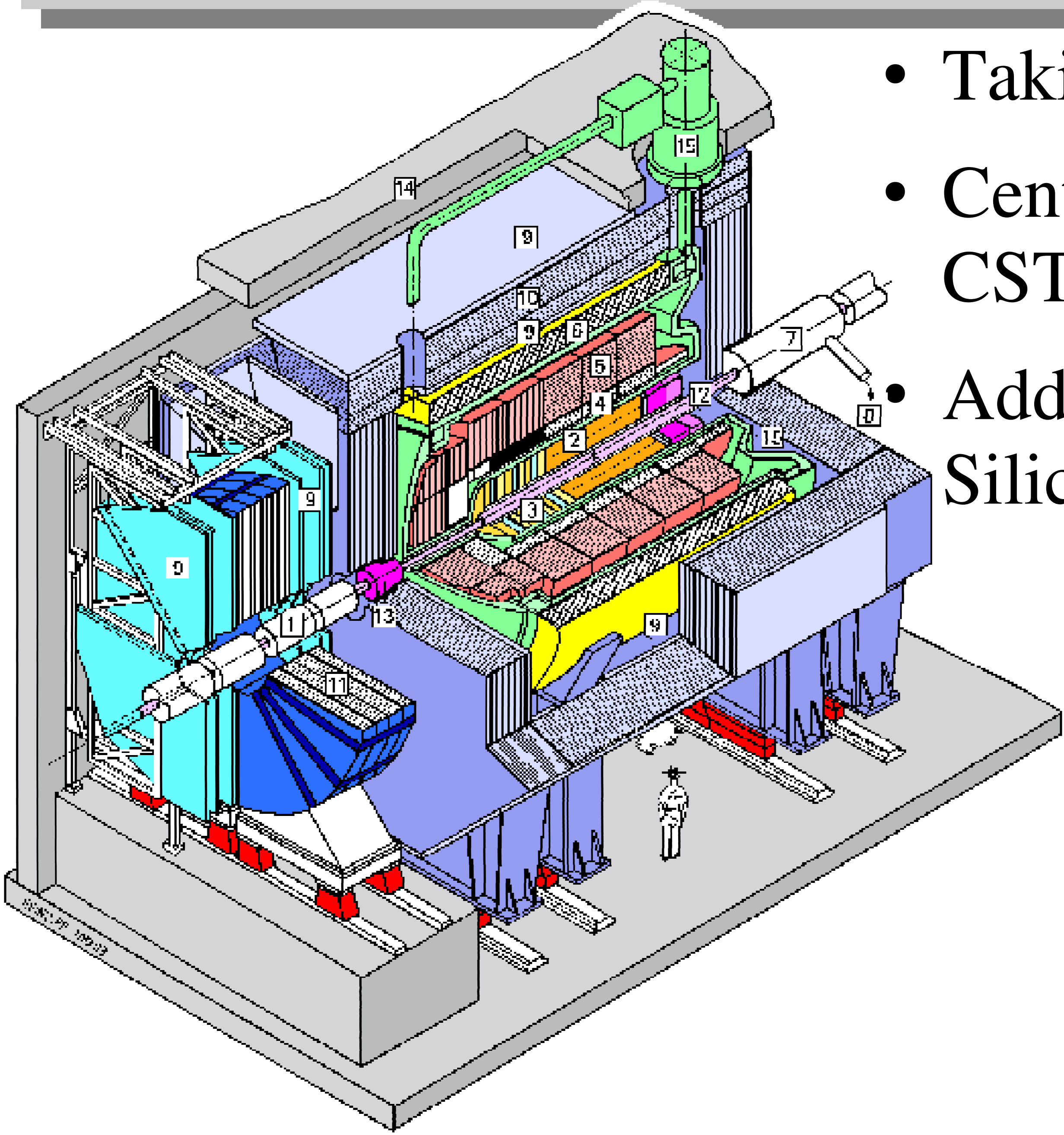
Introduction: HERA

- ep–Collider at DESY
- 50 mA Electrons at 27.5 GeV
- 100 mA Protons at 920 GeV
- »Worst of both Worlds«
  - Synchrotron radiation:
    - Radiation problem itself
    - Heats the beampipe
  - 4 kHz/m proton gas collisions
- Bunch spacing
  96 ns = 1/10.4 MHz •

Introduction: The H1 Detector



- Taking data since 1992
- Central Silicon Tracker CST installed in 1995
- Additional Backward Silicon Tracker in 1995
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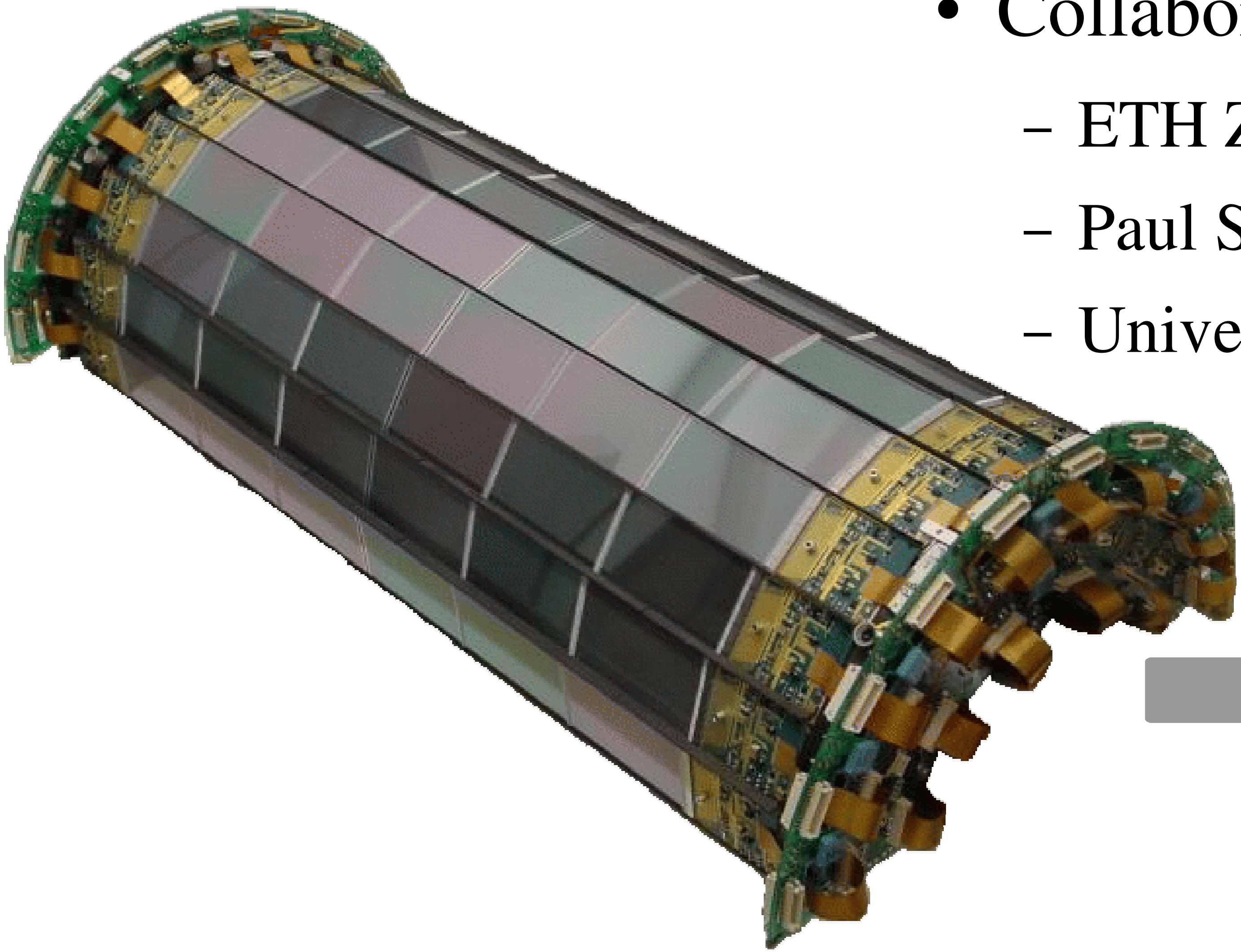
The H1 Central Silicon Tracker



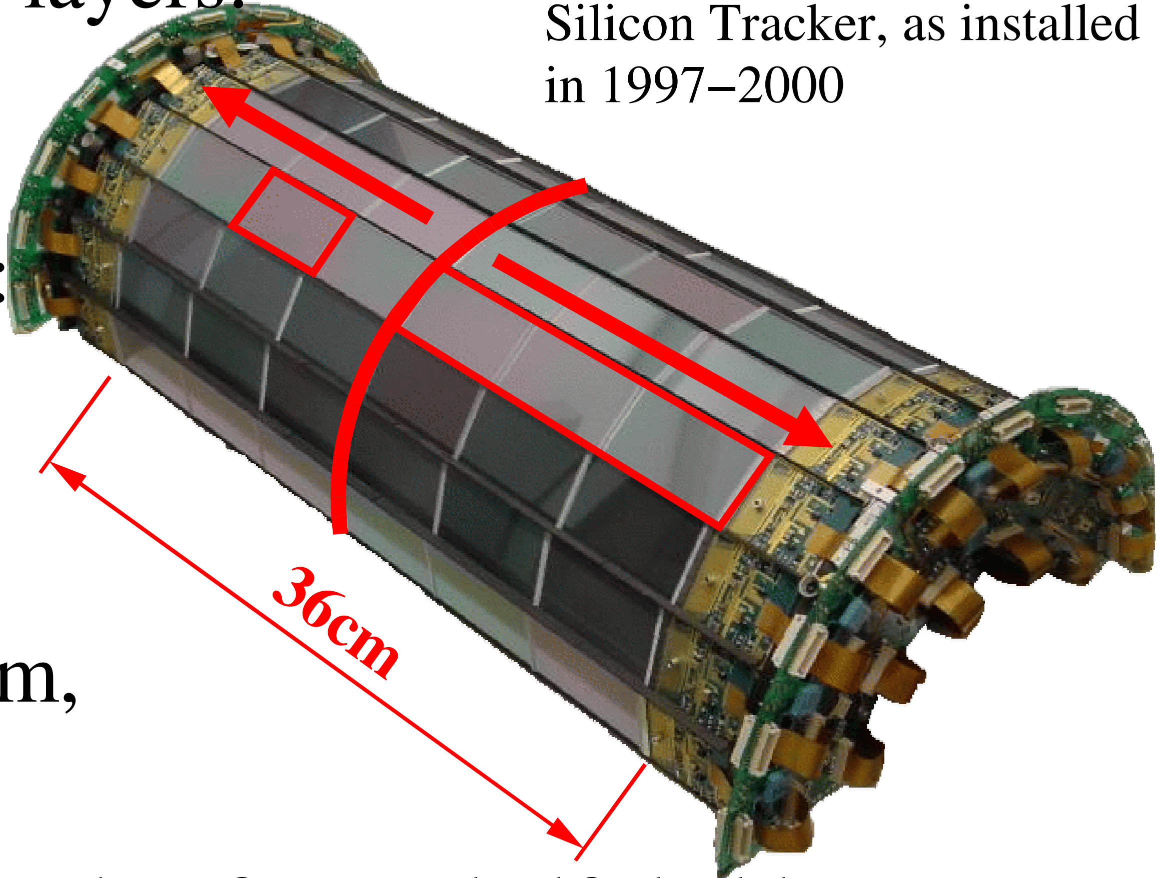
- Collaboration of
  - ETH Zurich
  - Paul Scherrer Institute
  - University of Zurich

The H1 Central Silicon Tracker

- 2 concentric (barrel) layers:

  6+10 ladders
  at radii of 6 and 10cm
- 6 sensors per ladder:

  size $5.9 \times 3.4\text{cm}^2$
  thickness $300\mu\text{m}$
  double sided
- Length: sensors 36cm,
overall: 60cm



One half of the H1 Central Silicon Tracker, as installed in 1997–2000

- 3 sensors bonded together form a half–ladder
- Readout on both ends•

H1 Central Silicon Tracker cont’d

- Charm and bottom at HERA: Typically small momenta (few GeV, single tracks <1GeV)
- Multiple scattering dominates impact parameter resolution
- Very little dead material:
  – $0.40 \mathrm{g/cm}^2 = 1.3\% X_0$
  – sensors: $0.16 \mathrm{g/cm}^2 = 0.7\% X_0$
- Covers $20^\circ < \vartheta < 160^\circ$

Downsides of readout at end:

- Inter−strip capacitance limits length and therefore angular acceptance
- Cannot place disks of Forward and Backward Silicon Trackers close to barrel sensors•

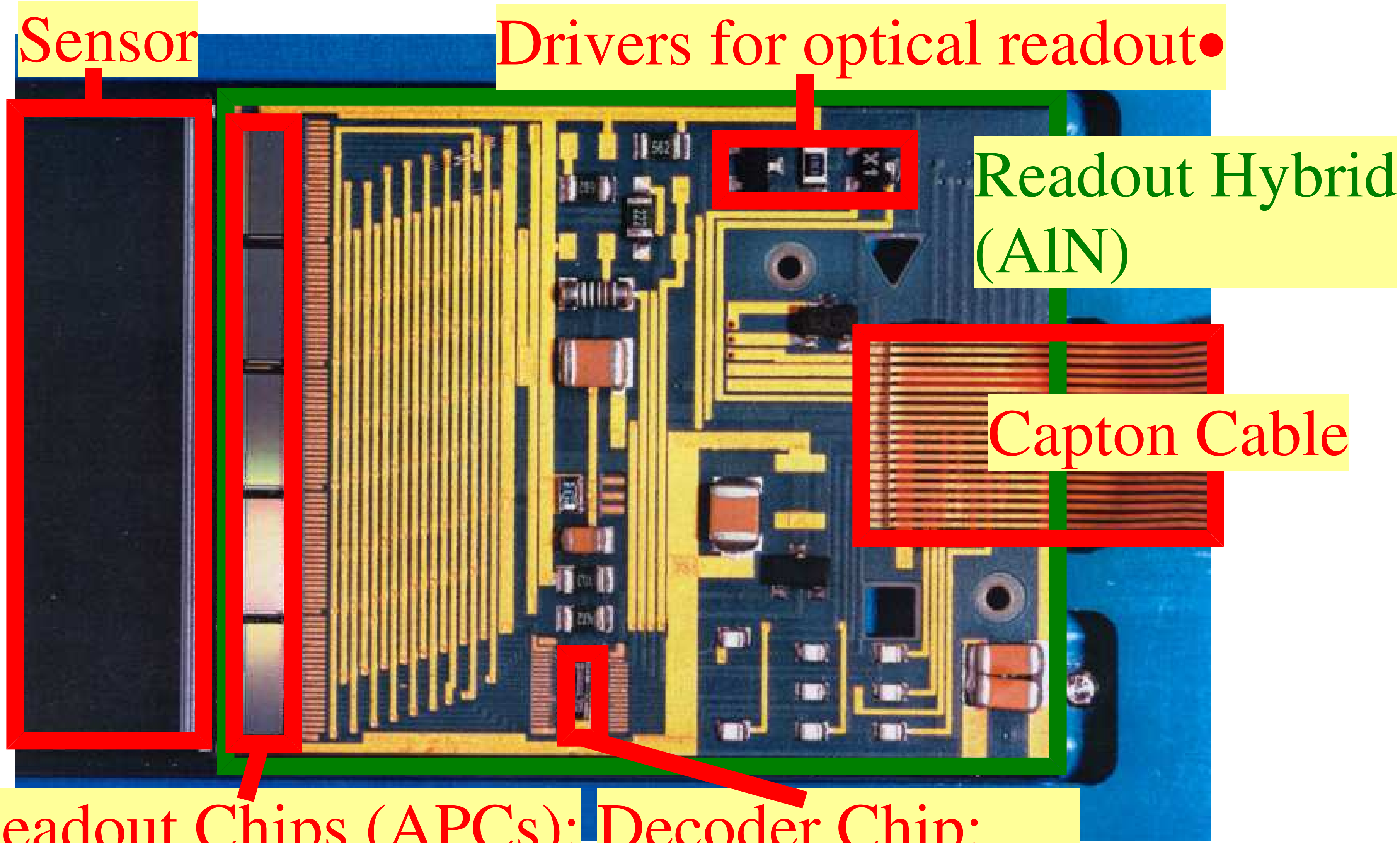
Sensors: Technical Data

- High resistivity (>6 kΩcm) silicon from Wacker
- Processed by CSEM
- area 5.9×3.4 cm^2, thickness 300 μm
- Double sided
- DC coupled
- 30–50V depletion voltage
- 3 sensors bonded together

- p Side:
  - 25 μm strip pitch
  - 50 μm readout pitch
  - 640 strips
  - 3×9 pF / strip
- n Side:
  - 88 μm pitch
  - 640 strips
  - 3×19 pF / strip
  - double metal •

Readout Hybrid

W. Erdmann et al.: NIM **A372** (1996) 188.



Readout Concept

- Total: 81920 channels
- Power consumption: ~50W (mostly preamps)
- 64 optical readout lines,
  each reads out 1280 channels in ~1.2ms
- Analog optical data transmission over ~30m from front end to electronics trailer
- Convert signals back to analog electrical signal
- 8 Power PC boards (CPU 68040) with custom add–on ADC board (built by Rutherford Labs) perform data processing (zero suppression & hit finding)•

W. Erdmann et al.: NIM **A372** (1996) 188.

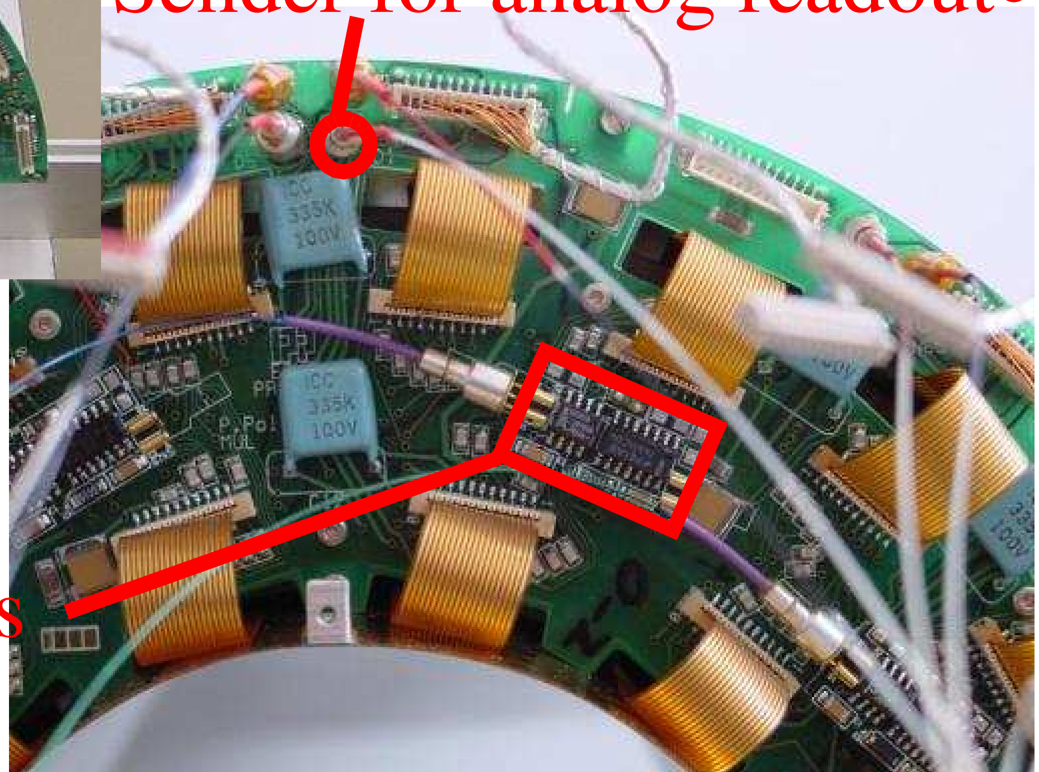
Endring Prints

Endring Print:
Distributes signals and power

Readout Hybrid

Capton Cable

Sender for analog readout•



Power Connectors

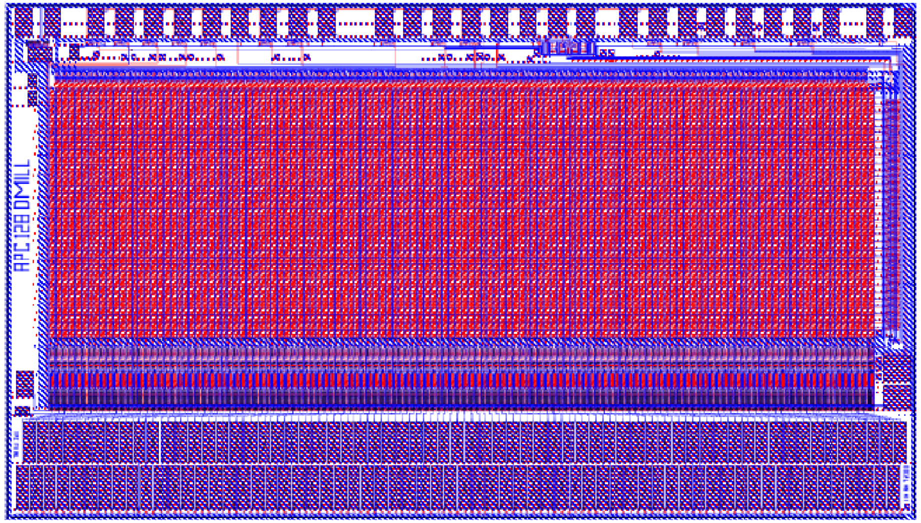
Filter Capacitors

Receiver for steering signals

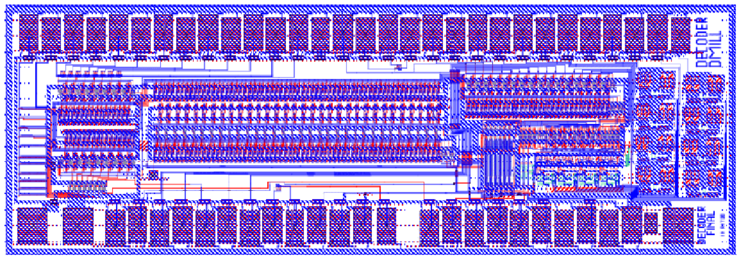
Readout Chips

2 ASICs, developed at Paul–Scherrer–Institute:

- APC128: Analog Pipeline Chip
  - 128 Channels
  - 32 stage analog pipeline
  - Buffers data at >10MHz
  - Serial readout at 2.5 MHz
  - $6.4 \times 3.8 \mathrm{mm}^2$



- Decoder:
  - $3.4 \times 1.3 \mathrm{mm}^2$
  - Provides Steering Signals for APC



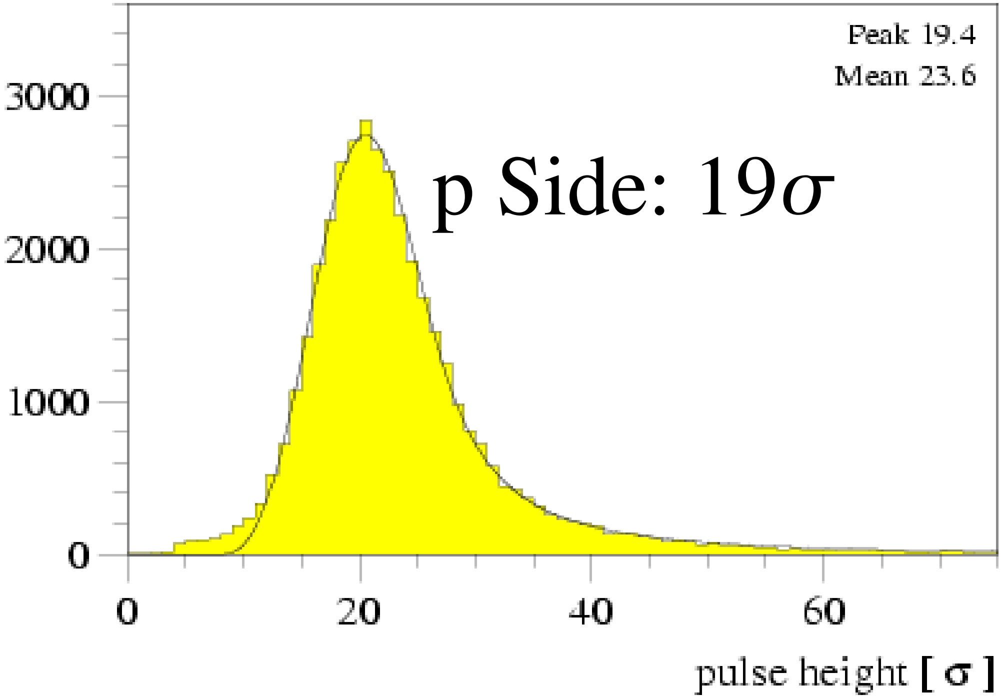
R. Horisberger, D. Pitzl: NIM. **A326** (1993) 92.

M. Hilgers, R. Horisberger: hep–ex/0101023.

Performance

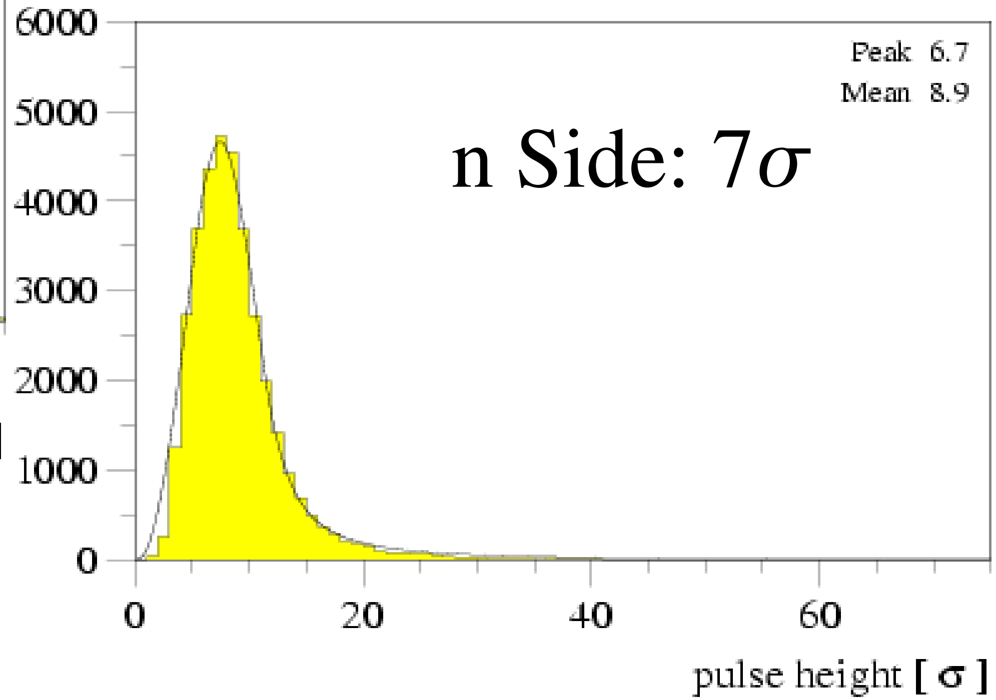
Signal/Noise: Measurement from penetrating cosmics

Total signal, divided by mean single strip noise



p Side: 19σ

D. Pitzl et al.: NIM **A454** (2000) 334–349.



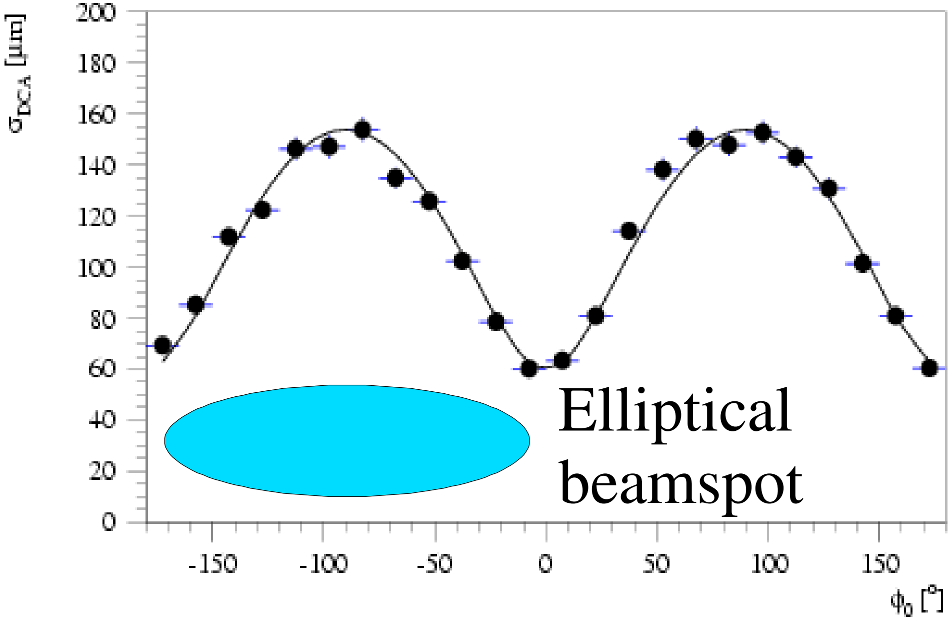
n Side: 7σ

D. Pitzl et al.: NIM **A454** (2000) 334–349.

Performance cont'd

- 4/128 half modules dead due to connector problems
- Hit finding efficiency (corrected for accidental noise and 3% loss due to gaps in z):
  - 98% on p side (measures $r\varphi$ coordinate)
  - 92% on n side (measures z coordinate)
- Problem on n side: Low signal to noise: $S/N_{\mathrm{strip}} \simeq 7$, but: typical cluster consists of about n=5 strips: $N_{\mathrm{cluster}} = \sqrt{n} \cdot N_{\mathrm{strip}}$
- Cluster cut: $S > 4 \cdot N_{\mathrm{strip}}$ results in 1 noise hit per 1.6cm on n side

Performance cont'd



D. Pitzl et al.: NIM **A454** (2000) 334–349.

Width of impact parameter distribution as measured with the CST as function of φ.

A fit gives:

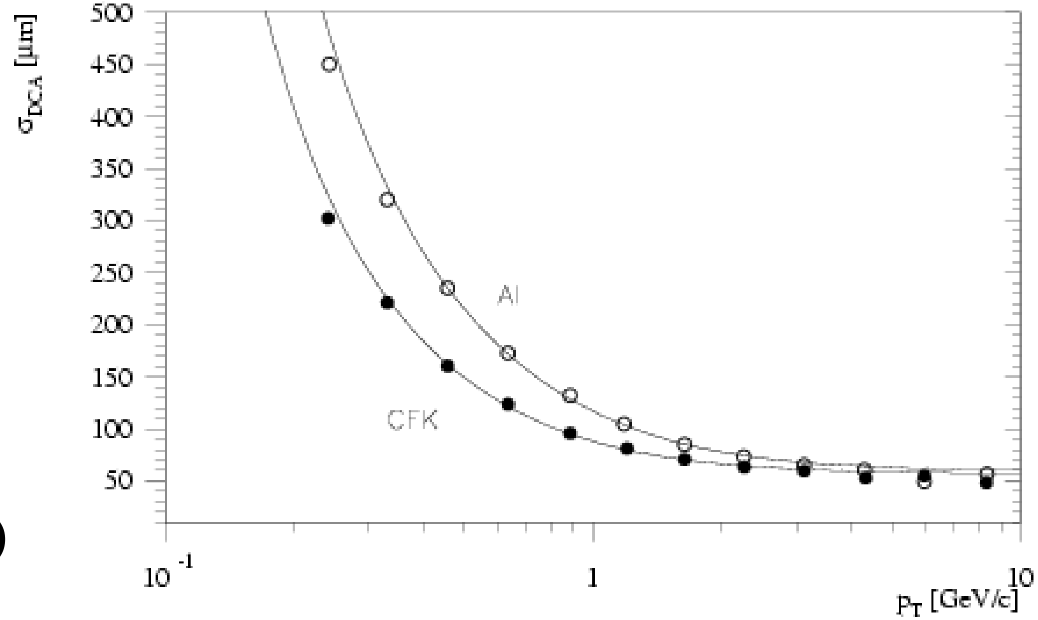
- Beamspot width: 155μm
- Impact parameter resolution: 54 μm.

CST impact parameter resolution as function of p_T.

❍ 1997: Al beampipe (1.9%X_0)

● 1999: Carbon beampipe (0.6%X_0)

Asymptotic resolution: 57μm

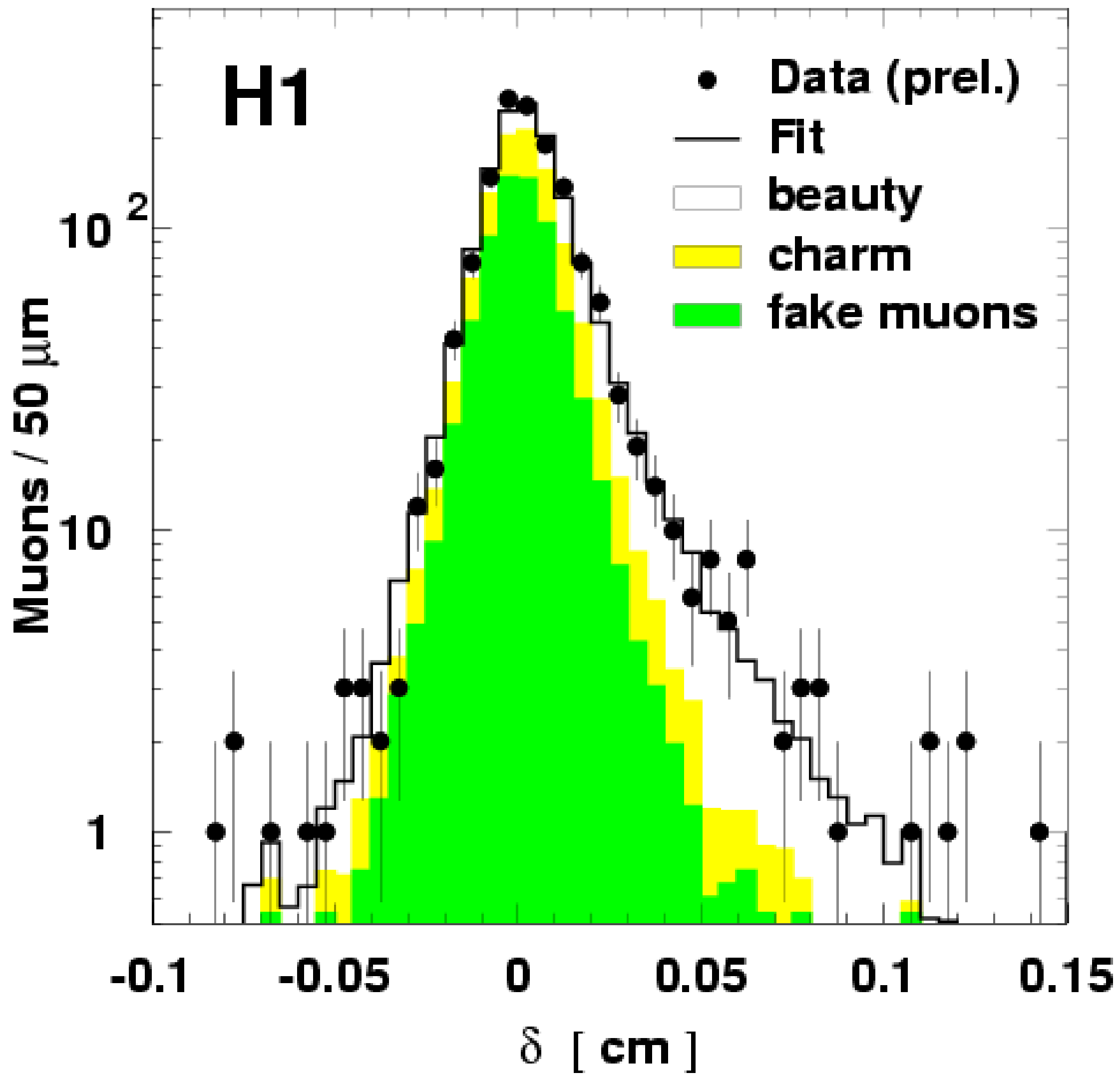


D. Pitzl et al.: NIM **A454** (2000) 334–349.

Performance cont'd

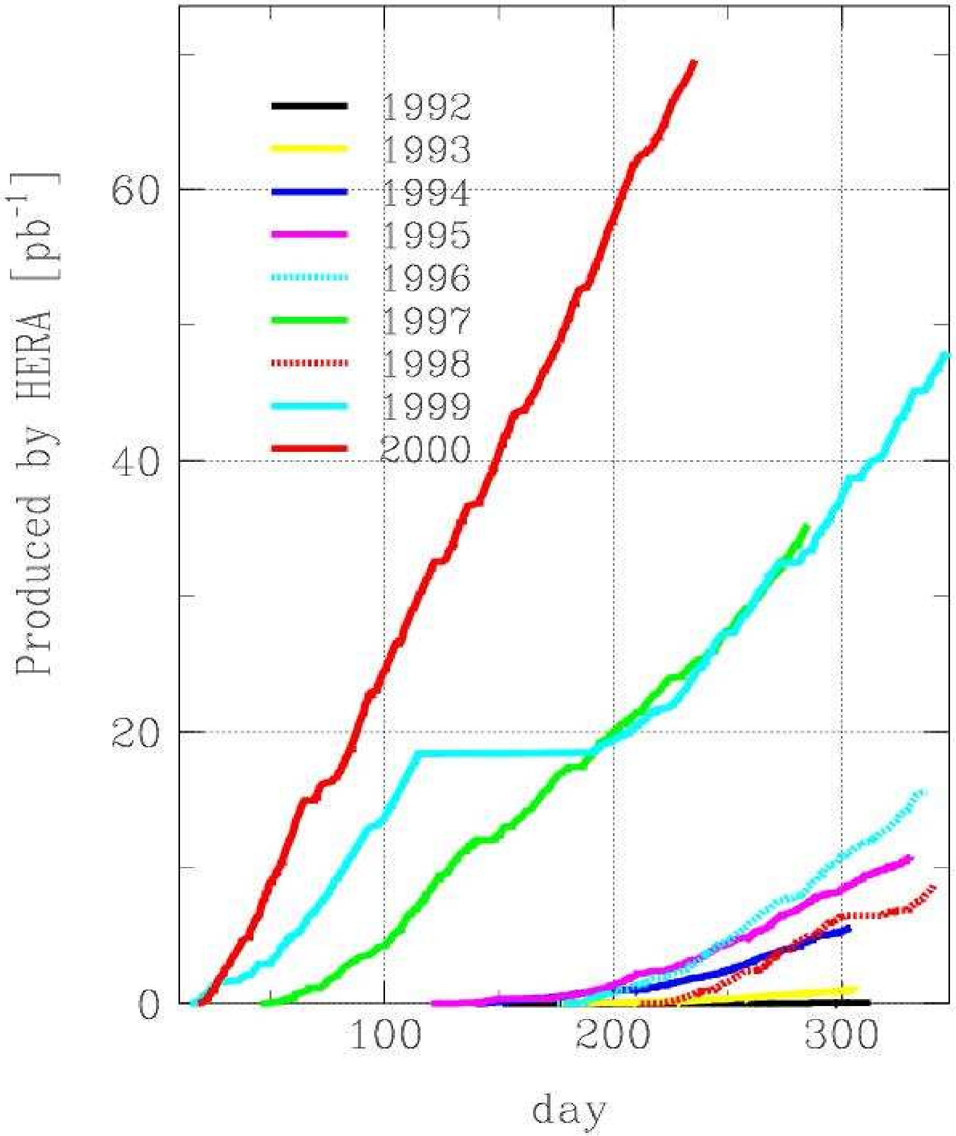
Measurement of Beauty production cross section:

- 2 jets E_T>5GeV
- 1 muon p_T>2GeV
- Look at impact parameter of muon ⇒
- Clear lifetime signal •



H1 Collaboration: Abstract 979, submitted to the 30th International Conference on High Energy Physics, ICHEP 2000, Osaka, Japan, July 2000.

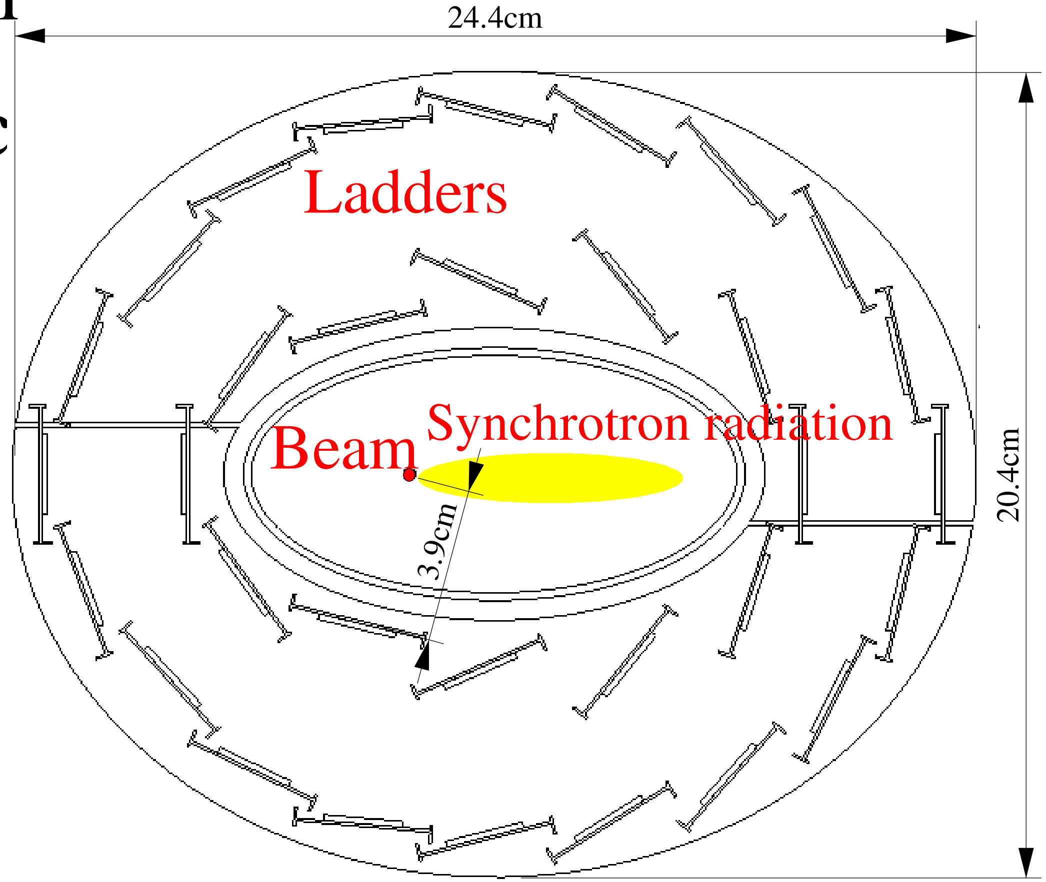
The HERA Luminosity Upgrade



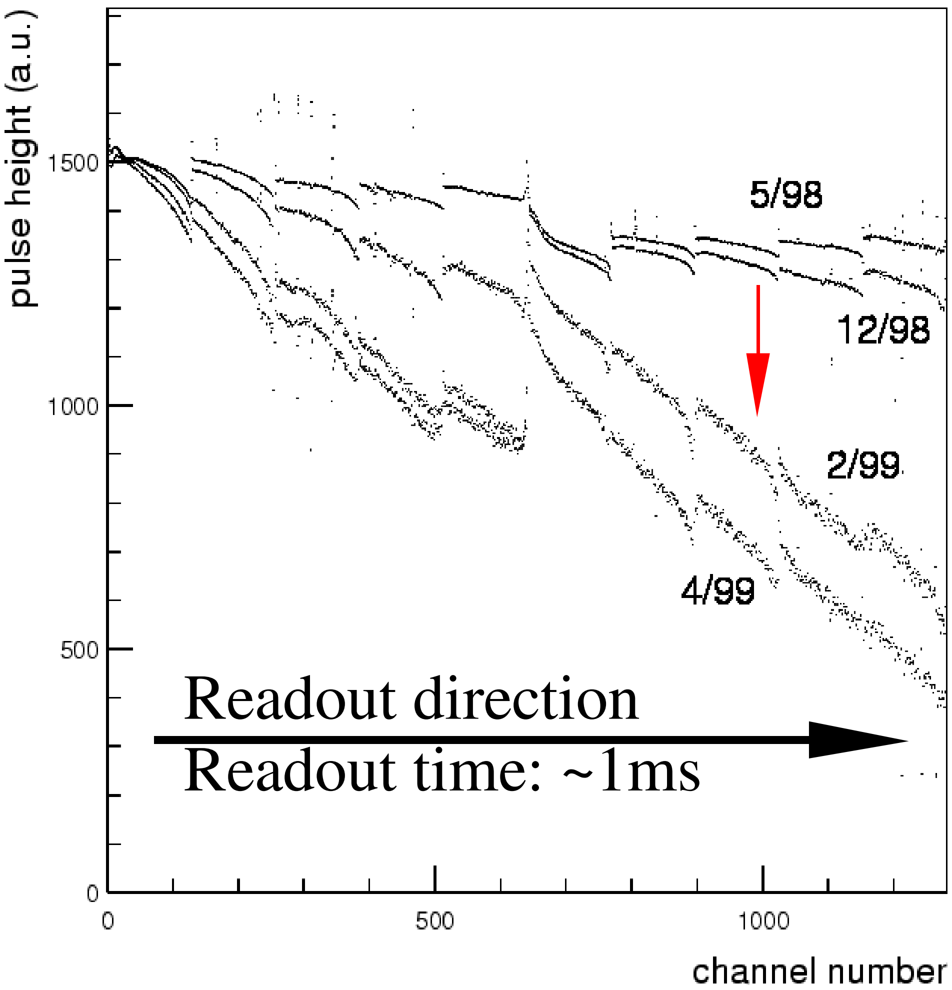
- HERA running since 1992
- Has delivered 185pb^{-1}
- Since Sept 2001: Upgrade underway: Increase lumi by factor 4: Beamspot decreases from $150 \times 40 \mu m$ to $80 \times 20 \mu m$
- New magnets inside H1
- New beampipe:
  - elliptical
  - not concentric•

New Ladder Arrangement

- Beampipe elliptical for synchrotron radiation fan
- Beampipe not symmetric around beam axis
- 2 Sensor layers
- Sensors perpendicular to rays from interaction point
- Overlaps in $r\varphi$ for internal alignment •



Radiation Damage



M. Hilgers, R. Horisberger: hep–ex/0101023.

- Beginning of 1999: about 25krad Synchrotron–Radiation received
- Problem: Internal leakage currents in the readout chip are accumulated during readout time of ~1ms
- Decision: Build new, radiation hard chips in DMILL technology•

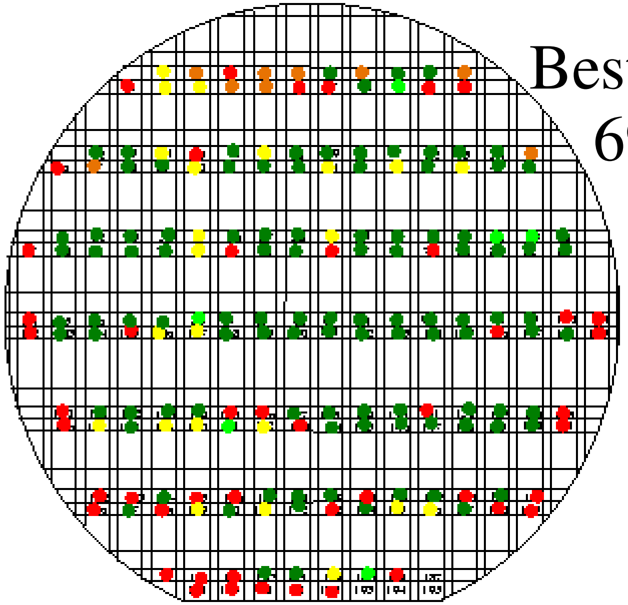
DMILL Technology

- DMILL: Durci Mixte sur Isolant Logico–Linéaire
- Developed by CEA (Saclay), licensed by ATMEL
- Bipolar CMOS technology, 0.8μm feature size
- Silicon on Insulator (SOI)
- 2 Metal Layers, 1 Polysilicon
- Radiation hard up to 10Mrad
- Components have the same footprint as in SACMOS1 technology (1.2μm feature size)

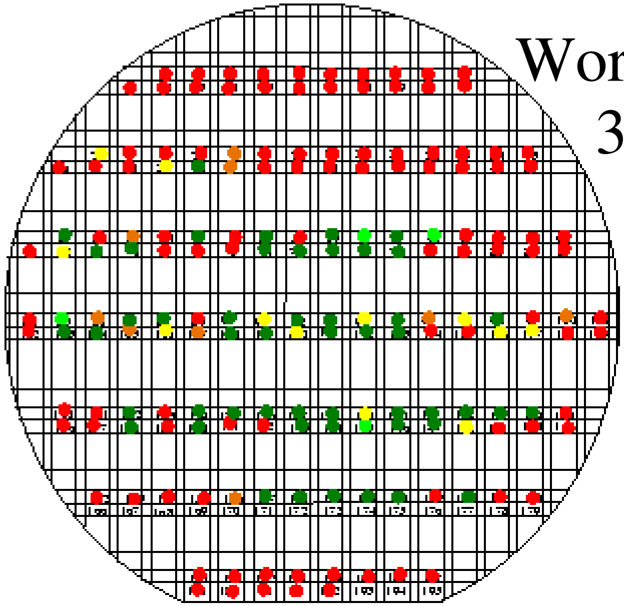
The DMILL Project

- May 1999: Decision to produce new readout chips in DMILL technology
- Sept. 1999: First prototypes submitted
- Mar. 2000: Prototypes back
- Aug. 2000: Final design submitted
- Mar. 2001: Chips delivered:
  - late delivery (export license problems)
  - only 5 wafers delivered (8 ordered)
  - low yield
- Replaced chips on 26/32 ladders
- Apr. 30, 2001: Installation of CST•

Yield



Best yield: 69%



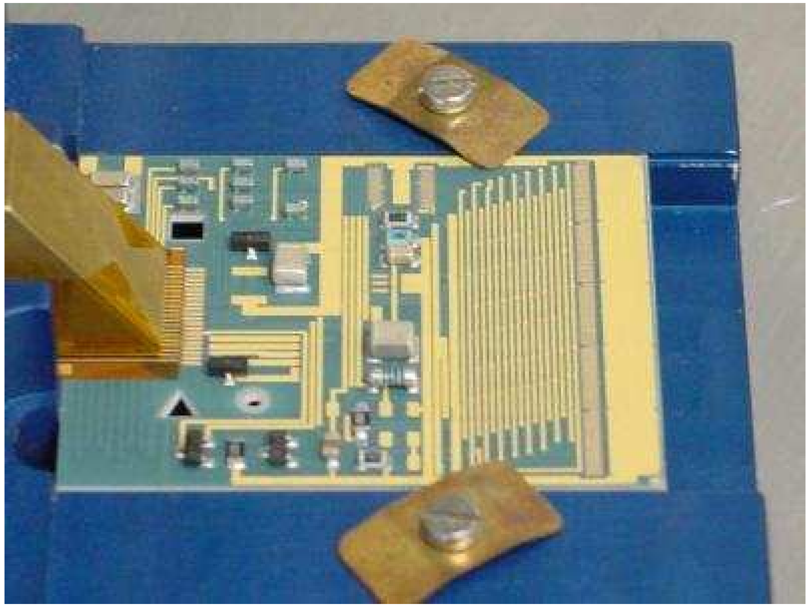
Worst yield: 37%

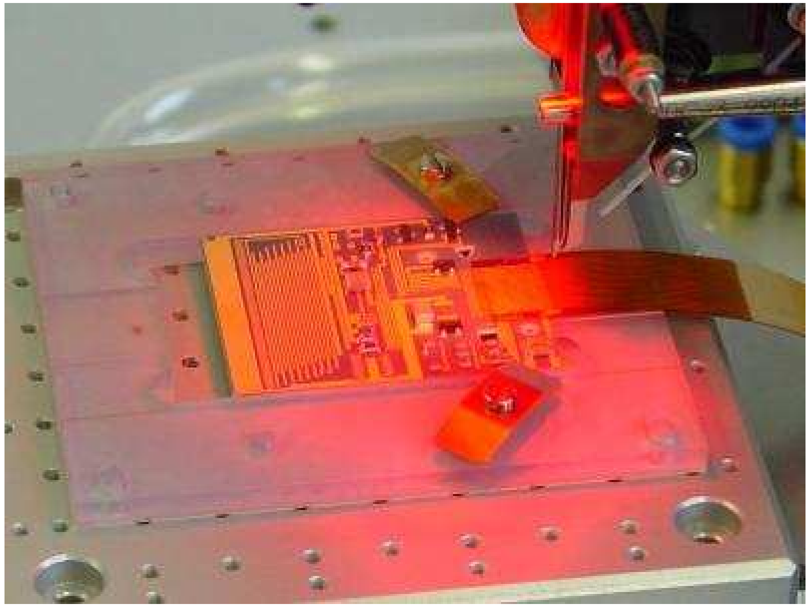
- Yield:56% for all 5 wafers
- Varied between 37 and 69%
- Accept 1 defect channel out of 128, or several defect buffers out of 4096
- Biggest problem:
  Defect dynamic shift registers
- Leakage currents on chips?•

Reusing the Silicon

- Goal: Replace the frontend readout chips
- Sever readout hybrid from silicon
- Remove 1280 bonds for each hybrid:
  - glue bonds to readout chip on hybrid
  - tear off hybrid: 95% of bond wires go off
  - bond pads generally not reusable

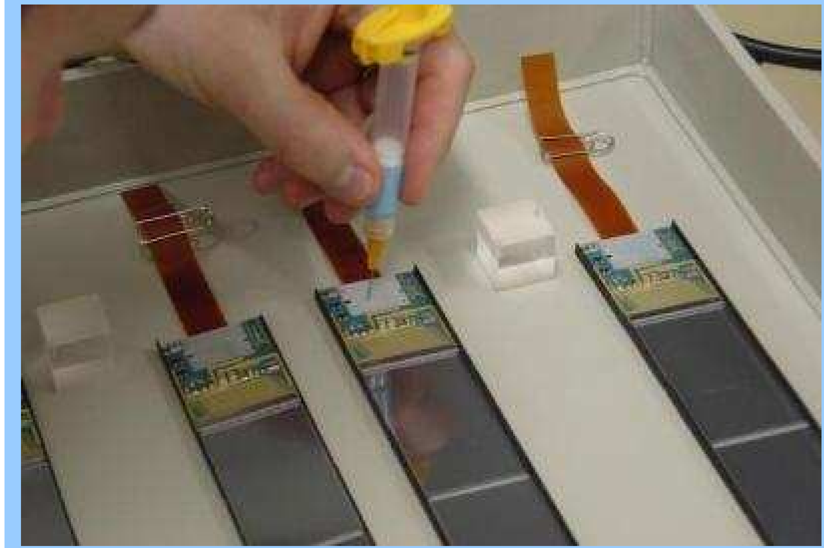
Hybrid Assembly



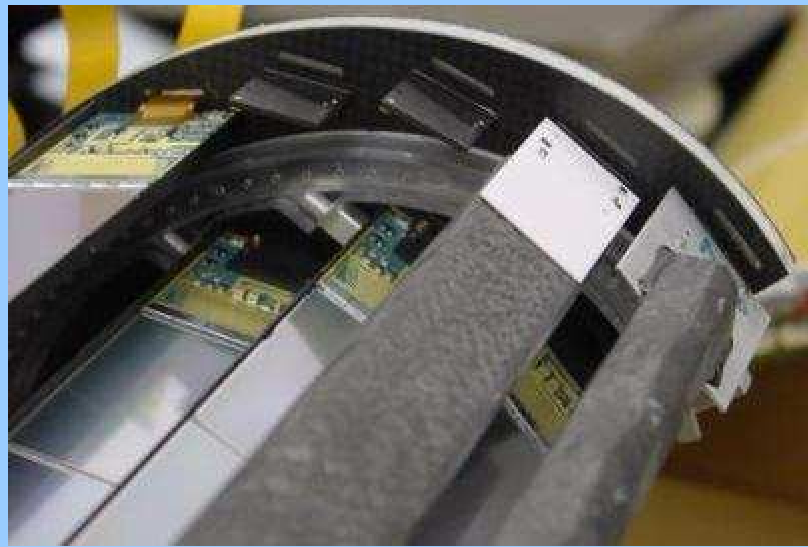


- AlN hybrids:
  good heat conductivity ⇒
  hard to solder
- Mounting and soldering of discrete components by external company:
  cheap @ good quality
- Too few chips delivered:
  Repairing 20% defect hybrids took 50% of our time

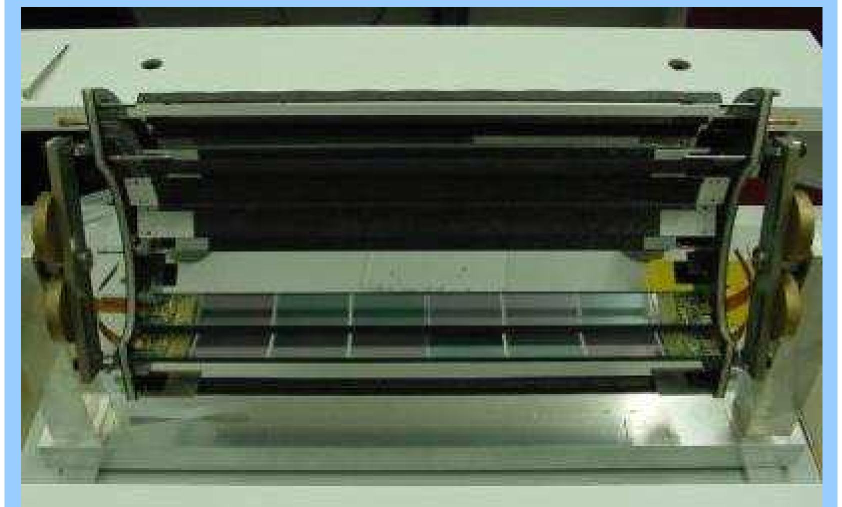
Assembly of the CST at PSI



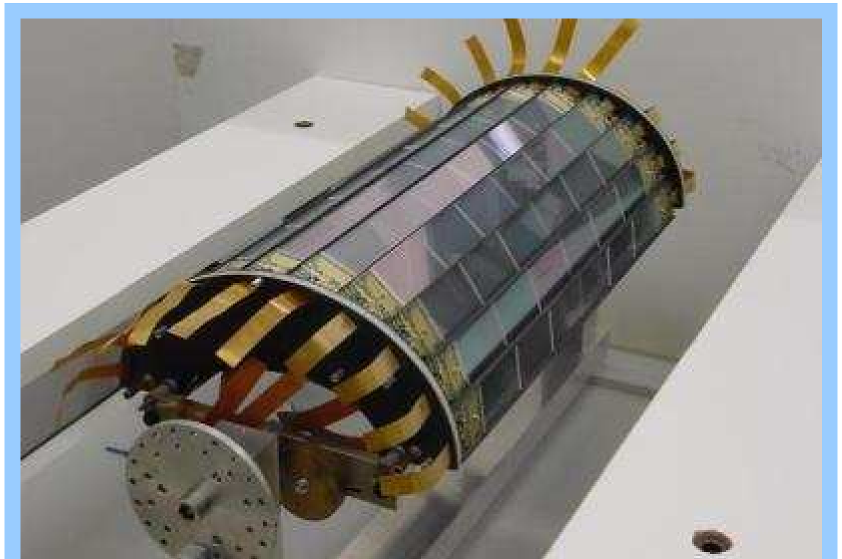
Application of heat−conducting paste



During assembly, dummy »ladders« are replaced by the real ones



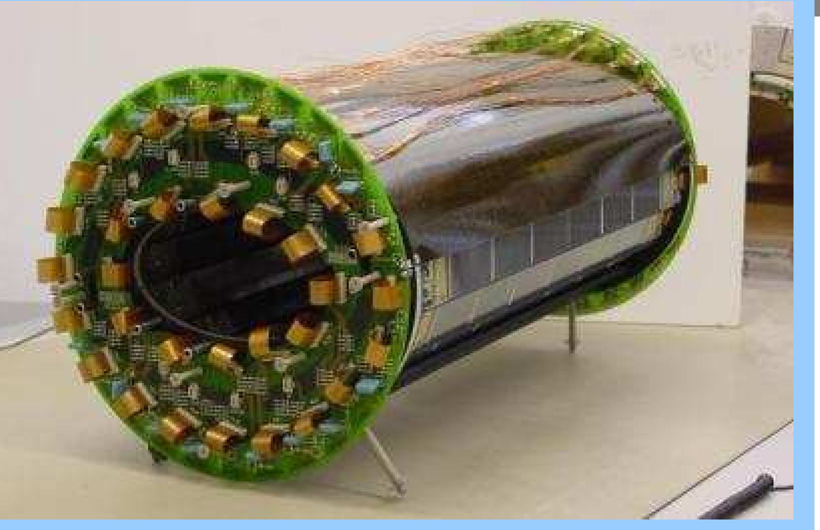
Special rotateable assembly frame



One half has been assembled

Assembly at PSI cont'd

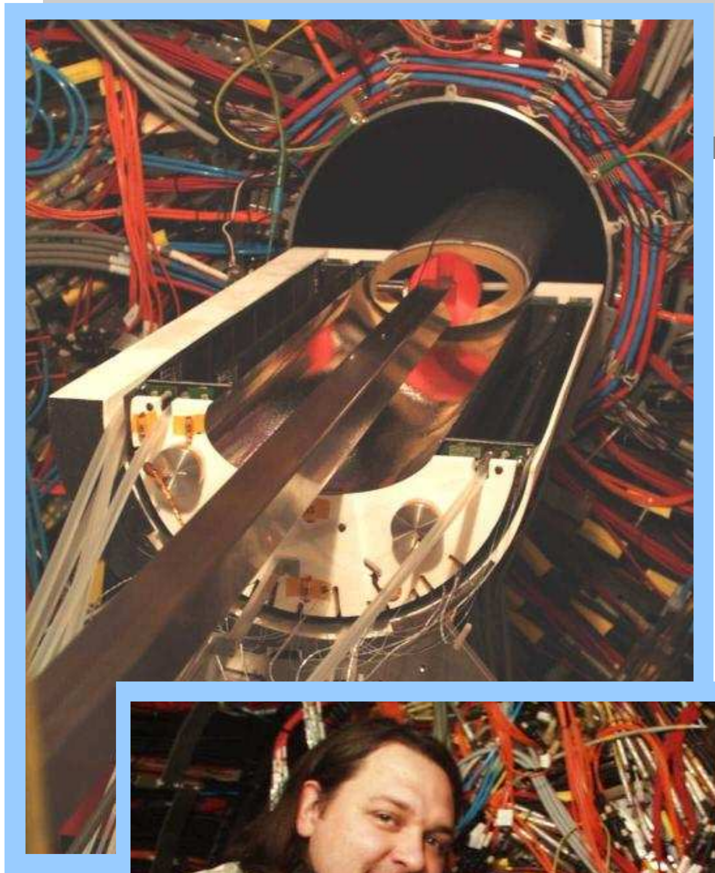
Endring Prints have been mounted

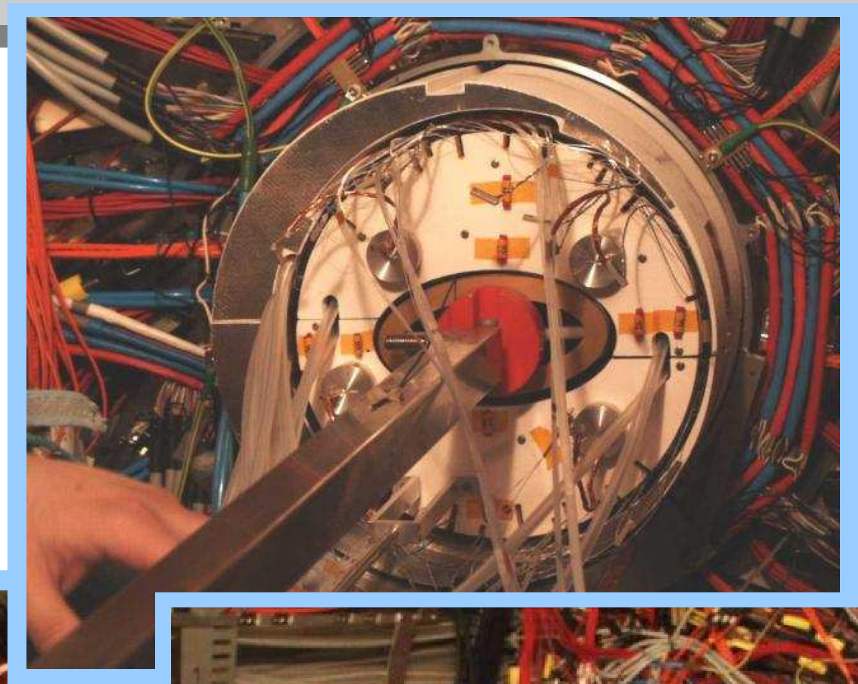


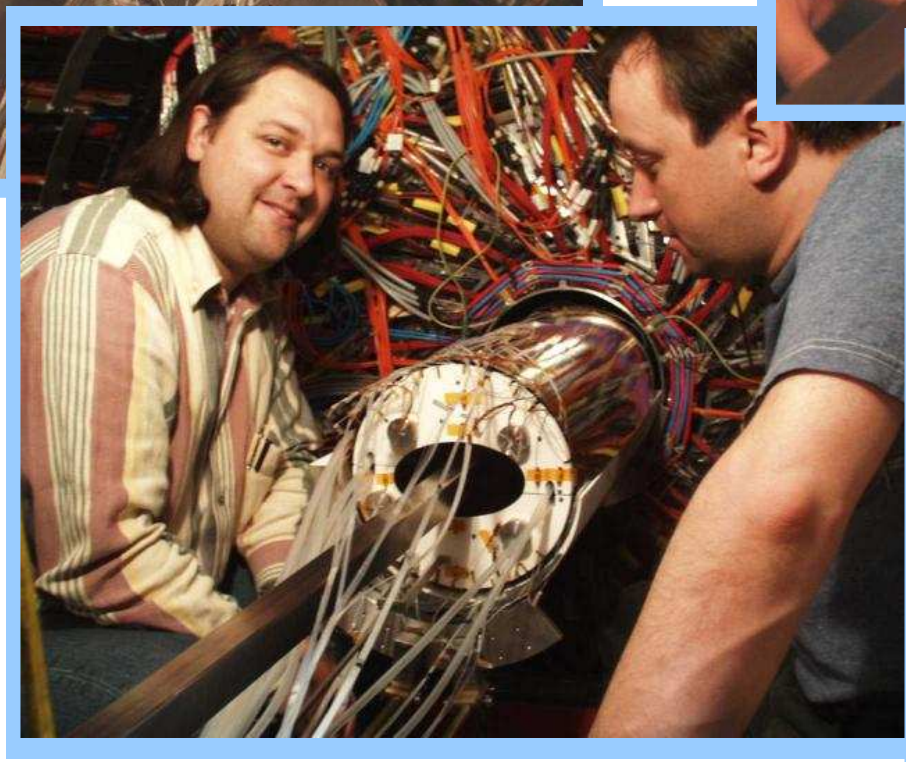
Both halves together

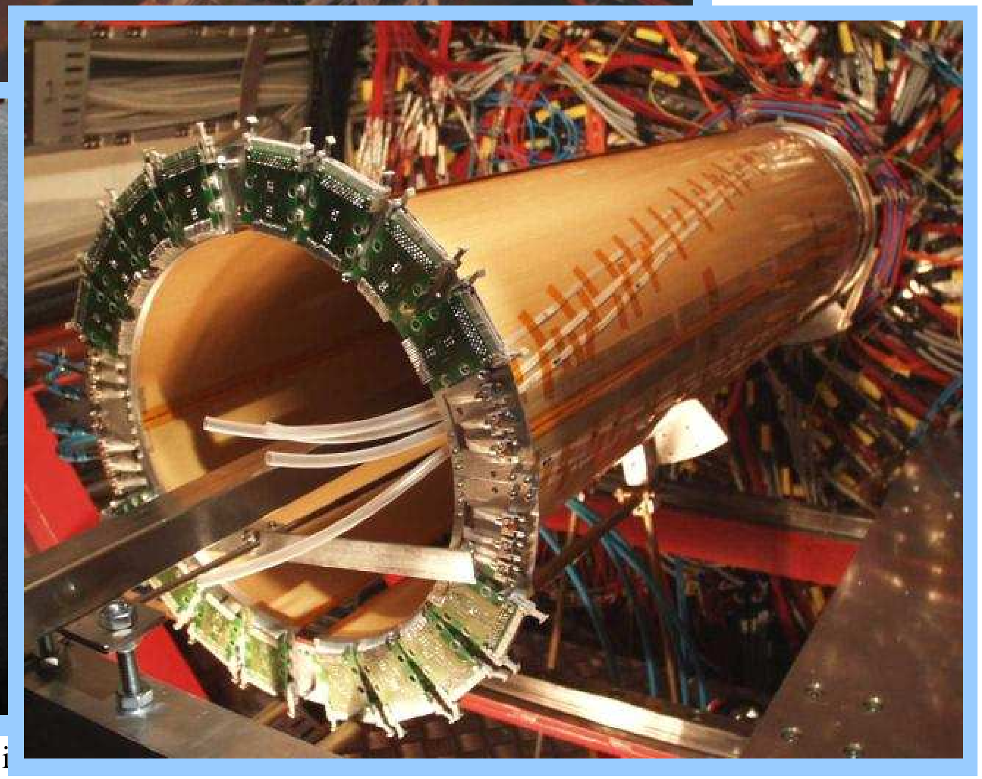
Both halves assembled; on right: power cables from back to front

Insertion

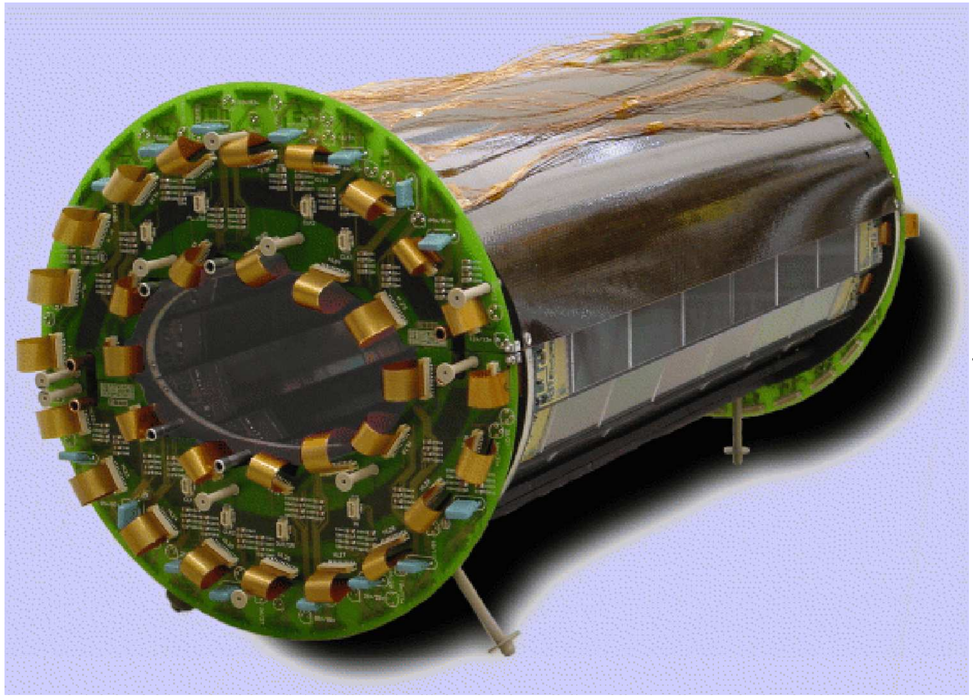








Summary



- CST of H1 operational since 1997
- Double–sided readout, 80k channels

Upgrade in 2001:

- Elliptical shape
- Radiation hard chips:
  - Reuse silicon sensors
  - Transfer ASIC design to new technology
- Start data taking end 2001•

Lessons

- Plan for 10–20% dead modules:
  Repair takes much time
- Each connector is a risk
- Cooling is crucial
- Stable power consumption:
  Draw the same current all the time (common mode!)
- Silicon is pretty robust
- Input protection on chips is important and helpful