The H1 SPACAL Time-to-Digital Converter System†

Eric Eisenhandler, Murrough Landon, Graham Thompson
Physics Department, Queen Mary & Westfield College, University of London, UK

John Dowell, John Garvey, Tim Nicholls
School of Physics and Space Research, University of Birmingham, UK

Phu Cam, Brian Claxton, John Dowdell, Viraj Perera, Steve Quinton
System Design Group, Electronics Division, Rutherford Appleton Laboratory, UK

Abstract

This paper describes a pipelined 1400-channel Time-to-Digital Converter (TDC) system for the H1 Scintillating Fibre Calorimeter, which will soon be installed in the H1 experiment at DESY. The main task of the TDC system is to determine the time of arrival of energy depositions, and send this information from bunch crossings that satisfy the event trigger into the H1 data acquisition system.

In addition, the TDC system must monitor the timing trigger, which vetoes bunch crossings that contain too much background energy. Products of the interaction are separated from background on the basis of their different times of arrival with respect to the bunch crossing clock. For this monitoring the TDC system uses automatic on-board histogramming hardware that produces a family of histograms for each of 1400 channels.

The TDC function is performed by the TMC1004 ASIC. The system digitises over a range of 32ns per bunch crossing with 1ns bins and a precision of 1ns. Because of the way the TMC1004 is designed, it is possible to vary the size of the bins between 0.6ns and 3ns by trading off measurement range for bin size. The system occupies two 9U VME crates.

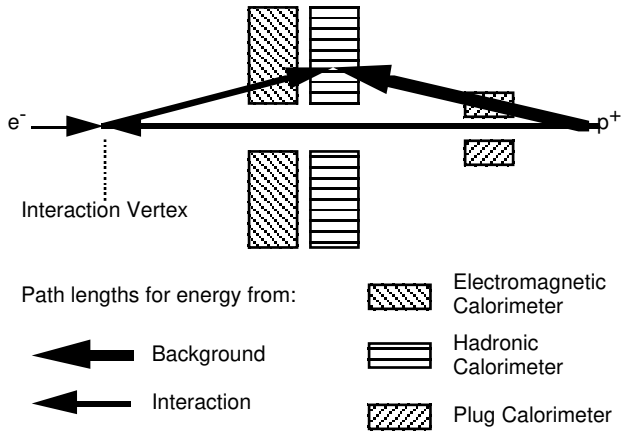

Figure 1 The SPACAL in H1

I. INTRODUCTION

The three sections of the H1 Scintillating Fibre Calorimeter (SPACAL) calorimeter [1] will be situated in the 'backward' region of H1 (upstream of the interaction point with respect to the proton beam), as shown in figure 1. Installation is scheduled for early 1995.

The calorimeter must provide precise measurements of the position (≤ 1mrad) and energy (~2% at 30 GeV) of electrons that are scattered off the proton at small angles in HERA, as well as a veto against background travelling with the proton beam. The second requirement is due to the fact that SPACAL replaces a dedicated Time-of-Flight Hodoscope [2] that is currently responsible for vetoing 99% of first-level triggers.

Proton-induced background (mainly due to beam-gas and beam-wall interactions upstream of the experiment) is distinguished from particles coming from the interaction by its time of arrival with respect to the bunch crossing clock (96 ns

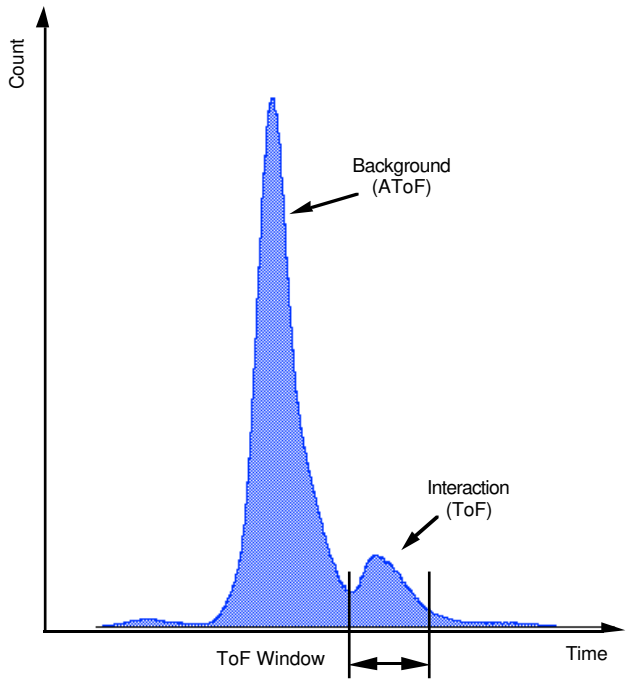

Figure 2 Histogram of the time of arrival of energy

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period). Because of the position of the SPACAL, proton-induced background will reach the calorimeter before the products of the interaction by twice the time of flight from the calorimeter to the interaction region — about 9ns in the case of the electromagnetic section. This is shown in figure 2; note that there are considerably more depositions of energy from background sources than interaction products.

For each channel in the SPACAL front-end electronics there is a 'ToF window', whose width and phase with respect to the bunch crossing clock is programmable. Energy that arrives within this window is referred to as 'in time' (ToF). All other energy is referred to as 'out of time' (AToF). From this information a decision is taken to veto a bunch crossing if too much energy arrives out of time (i.e. there is too much background).

Such a veto is necessary because of the high backgrounds associated with the proton beam. These large sprays of background can fool the track triggers, causing a first-level trigger and readout of data. This is undesirable since the trigger rate is needlessly high, and events with a large number of tracks produce a large volume of data, and hence take longer to read out. They therefore contribute in several ways to experimental deadtime.

To measure both energy and timing, the type of calorimeter chosen was a SPACAL (SPAghetti CALorimeter). This device is constructed of lead sheets with scintillating fibres laid in grooves. The ratio of lead to scintillator (2:1) is chosen to optimise the electron and photon energy resolution and to allow clean detection of minimum-ionising particles. The use of phototubes allows a time resolution of less than or equal to 1ns to be achieved. The phototubes must work in a 1T magnetic field, and so special mesh-dynode ones are used.

The Time to Digital Converter (TDC) system digitises the time of arrival of energy depositions and is subsequently read out by Digital Signal Processors (DSPs). It also produces histograms that are used for setting up the front-end electronics and subsequently monitoring it. This is important to ensure that the number of good triggers that are erroneously discarded — and bad ones that are allowed — is small. These histograms can also be used to monitor beam conditions, as the present scintillator hodoscope does.

Because of the short bunch-crossing interval in HERA, the entire TDC system must be pipelined during the latency allowed for first-level triggers, which is 2.5μs.

II. THE TMC1004 CHIP

This device was designed as a prototype of readout electronics for trackers at SSC and is now commercially available. It has been described in detail elsewhere [3,4].

A conceptual diagram of the device is shown in figure 3.

The TMC1004 digitises the time difference between a clock and a timing input. Each chip contains four channels with individual timing inputs and a common clock.

The digitisation is performed using a chain of thirty-two delay elements controlling the write input to a chain of

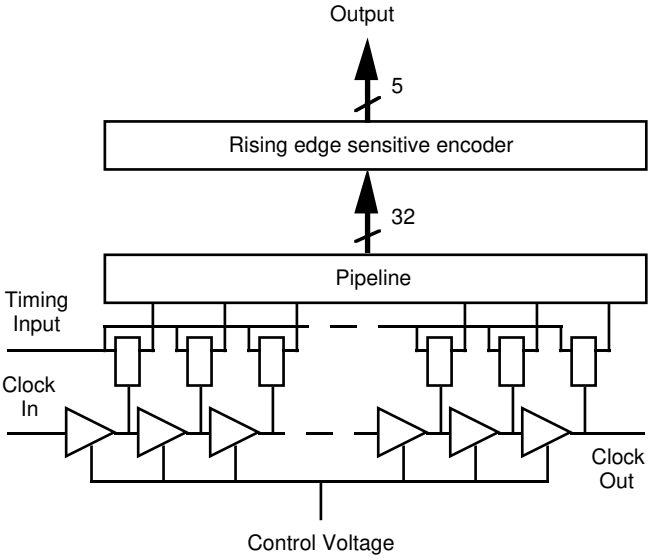


Figure 3 Conceptual view of the TMC1004 chip

memory cells. The timing input is connected to the data input of all memories. A clock edge propagates down the chain of delay elements, storing the state of the timing input in the memory at intervals given by the delay of the delay elements.

The position of a zero to one transition in the data stored in the memories indicates the time between the rising edge of the clock and timing input.

The delay of the delay elements is dynamically controlled using a control voltage. If the input and output clocks are not in phase a phase-locked loop (PLL) either increases or decreases the control voltage until they are. In this way the delay per stage is controlled to be one thirty-second of the clock period.

The precision of the TMC1004 alone is specified to be 0.5ns.

This means that the 'bin size', or accuracy of the TDC measurement, can be varied by varying the clock frequency, a feature used in this system. The range over which the control of the delay is guaranteed is 0.6ns to 1.5ns (corresponding to clock frequencies of 50MHz and 21MHz respectively).

The device also contains a pipeline for storing the data for a number of clock cycles. This is necessary because data must be stored until the first-level trigger decides that it should or should not be read out.

The pipeline is implemented as a circular buffer so its depth can be configured to be up to 32 clock cycles long, under the control of read and write pointers. The ability to change the pipeline length is used in this system to implement both the monitoring and data acquisition functions using a single channel of a chip.

III. System Description

A. System Architecture

The TDC system receives discriminated signals from all 1400 channels in the SPACAL detector. Because of the large dynamic range in pulse height, constant-fraction discriminators are used.

The system is contained in two 9U by 400mm crates with standard J1 VME (A24 D16). A custom J2/J3 bus using five row DIN connectors allows for rear plug-up of all inputs and the fan-out of clock and control signals. The J2/3 bus also provides the private acquisition bus over which data is sent to the readout DSPs.

Figure 4 shows a block diagram of the system.

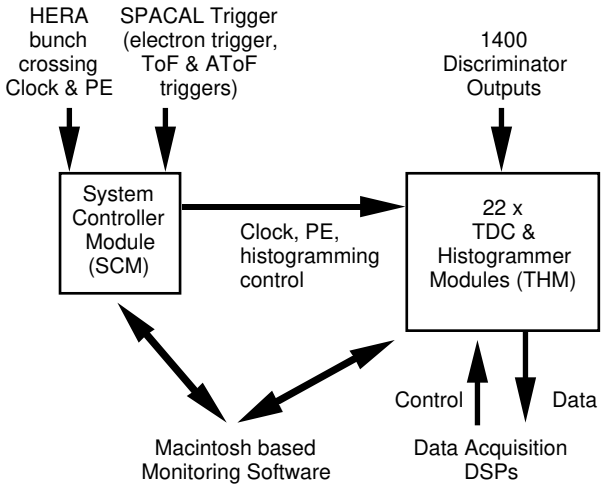


Figure 4 Block diagram of the TDC system

The TDC function is performed on twenty-two TDC and Histogrammer Modules (THMs), each with 64 channels (16 TMC1004 chips). These modules are connected to the front-end electronics using 23m of shielded twisted pair cable.

One System Controller Module (SCM) receives the central HERA bunch crossing clock (10.4 MHz) and the pipeline enable (PE). It multiplies the bunch crossing clock by a programmable multiple, between one and five but normally three, to produce the TMC clock. The TMC clock and pipeline enable are fanned out to all THMs on equal length cables.

The SCM also provides thirty-two bit scalers for use by the monitoring software (e.g. number of bunch crossings, number of pipeline enables, etc.). These are implemented in Xilinx XC3042s.

On-board histogramming of each channel is discussed in a later section.

The contents of the TDCs, scalers and histograms are accessible to a Macintosh-based monitoring program. The use of a private bus for communication with the DSPs allows the Macintosh uninterrupted VME access, even during data taking.

A block diagram of the THM is shown in figure 5. It will be discussed in the next sections.

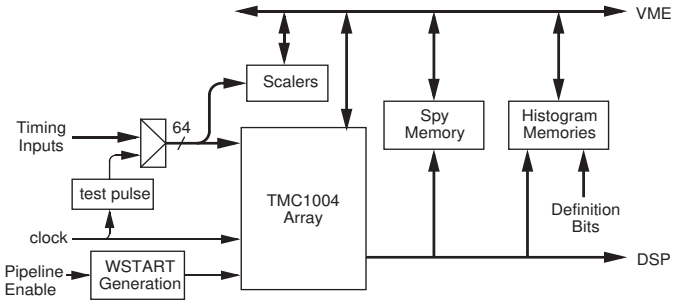


Figure 5 — Block Diagram of the THM

B. TDC Data Acquisition

While the pipelines are enabled, the TMC chips acquire the time of arrival of energy with respect to the TMC clock, for each channel. When a first-level trigger occurs (2.5μs after the bunch crossing of interest) the pipelines are frozen and data from the triggered bunch crossing (and one either side for safety) is accessible to calorimeter DSPs. Two DSPs situated in a remote data acquisition crate read the data over the private acquisition bus. Each DSP reads out one crate of THMs, zero suppresses the data and places them into a buffer for the event builder.

Consider the case of a TMC clock of 32ns period (one third the bunch crossing clock). The depth of the TMC1004 pipelines is 1μs if data are recorded continuously (32 times 32ns). If different clock multiples are used the pipeline depth varies proportionally. This will not accommodate the H1 trigger latency, therefore the pipelines must be extended.

The solution adopted, to avoid the use of external memories, is to record data from only one TMC clock cycle per bunch crossing. This extends the length of the pipelines to 3.2μs regardless of TMC clock period, which is adequate for the trigger latency.

Experience with the present time-of-flight hodoscope has shown that the full base width of the histogram in figure 2 is 32ns — therefore this compromise is acceptable. The phase between the bunch crossing clock and TMC clock can be adjusted to position the 32ns active window such that it straddles this histogram.

This trade-off means that precise measurements can be made only over small ranges, but crude measurements can be made over wide ranges. Table I shows the relationship between clock multiple, bin size and measurement range.

Multiple	TMC clock (MHz)	Bin Size (ns)	Range (ns)
1	10.4	3.0	96
2	20.8	1.5	48
3	31.3	1.0	32
4	41.7	0.75	24
5	52.1	0.6	19.2

Table I Trade-off of bin size versus range

Multiple three (1ns bin size, 32ns range) will be the standard mode of operation of the system. The other modes are intended for commissioning and other investigations.

Clock multiple one yields a frequency that is outside of the specification of the TMC1004, but tests have shown that most TMC1004s still operate in this region, though not as accurately. Multiple one can therefore be used for qualitative checks of the whole 96ns bunch crossing, which could be important during initial commissioning.

C. Input Rate Scalers

There is one thirty-two bit scaler per sixteen channels, implemented in a Xilinx XC3020. Individual channels can be gated on or off, so that these scalers can be used both to monitor overall rates in blocks of 16 channels and to set the threshold of the front-end discriminators just above the noise channel by channel.

D. Automatic On-Board Histogramming

The position of the ToF window in each channel will need to be set up initially and monitored periodically in case of drift in the analogue electronics. This will be performed using the on-board histogramming function of the TDC system.

It is also desirable to implement more complex monitoring functions. For example the number and time distribution of particles that pass the electron trigger could be histogrammed as a function of energy deposited in the electromagnetic and hadronic calorimeters.

This monitoring is based on the principle of producing a set of histograms, per channel, that show TDC value as a function of the global SPACAL trigger decision.

There are sixteen histograms per channel. Data from a given bunch crossing are added to the histogram specified in a set of four 'definition bits' — fanned out from the SCM.

The definition bits are generated from the SPACAL trigger bits (e.g. electron trigger, trigger on ToF and AToF energy sums, etc.) using a RAM-based look-up table. In this way, the significance of the histograms is completely programmable and can be changed to allow different investigations to be carried out.

There is one histogrammer per sixteen channels. Although only one of these channels is selected for histogramming at a time, all sixteen can be stepped through automatically.

The histograms are stored in RAM, requiring 1024 32 bit words per channel — giving a total of 5.5 Mb of histogram RAM in the system.

To histogram data from one bunch crossing takes eight bunch crossings (during which the histogrammer is insensitive), so not all cycles are histogrammed. With zero suppression this is acceptable, given the low occupancy of each channel. Insensitivity for several bunch crossings after a hit has the advantage that reflections in cables and perturbations in the analogue front-end electronics have time to decay without being histogrammed. Such effects have been observed in the present scintillator hodoscope.

These histograms are accessible to monitoring software, along with the scalers on the SCM and THMs, for on-line checks and expert diagnosis. It should be possible, for example, to write a program that can automatically align the ToF windows in the front-end electronics, using the delay lines provided on each channel.

To ensure that the on-board histograms are unbiased by the first level trigger, data are histogrammed as soon as they and the SPACAL trigger decision are available (of the order of 1μs after the bunch crossing to which both refer). This means that an event from a bunch crossing that ultimately fires the first level trigger has the same probability of being histogrammed as one that does not, and vice versa.

To pick off data at an intermediate stage in the TMC1004 pipeline, the write and read pointers are set up when the pipelines are enabled to the length required for histogramming. Data that pass the read pointer are not lost because the pipeline is a circular buffer, so when the pipelines are subsequently frozen by a trigger the read pointer can be reset to the level one trigger latency behind the write pointer and the triggered bunch crossings read out by the DSP.

IV. Results of Beam Tests

The performance of the system has been assessed during three test beam runs. The first two used pre-prototype hardware (no DSP readout or automatic histogramming) and the third final prototypes.

A. TDC Performance

The time precision of the TDC system has been measured to be approximately 0.80ns. This was determined using the difference between the time of arrival measured by the TDC system and the time of a beam trigger, as shown in figure 6. The latter was measured by a CAMAC TDC module with 0.1ns resolution.

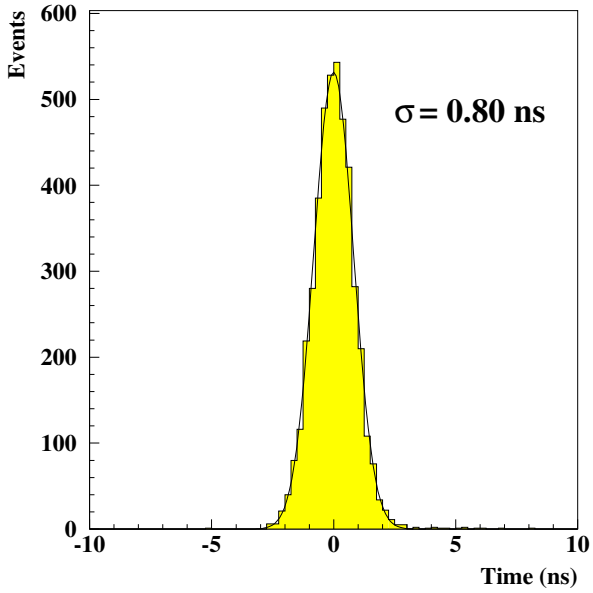
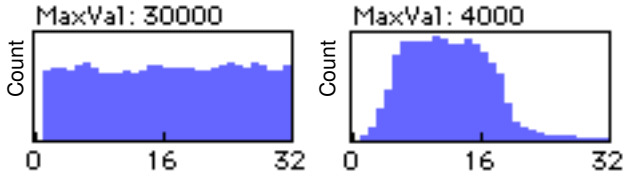


Figure 6 Precision of the time measurement

B. Automatic On-Board Histogramming

The function of the electron trigger is to select those particles whose energy depositions are greater than a given threshold in an area of four by four channels of the calorimeter and that come in time with the ToF window.

Figure 7.i shows a histogram of the time of arrival of energy in one tower with respect to an artificial bunch crossing clock acquired by the automatic histogramming for a beam containing pions and electrons. Because there is no relationship between the test beam (at the CERN PS) and the bunch crossing clock the distribution is flat.



i) Unbiased, beam containing electrons and pions.

ii) Requiring electron trigger, beam containing electrons and pions.

Figure 7 Histogram of TDC values acquired automatically, unbiased and requiring the electron trigger

Figure 7.ii was produced by the on-board histogramming when it was required that the electron trigger be satisfied in the same bunch crossing. This histogram shows the position and width of the ToF window in the artificial bunch crossing clock cycle, degraded by the resolution of the system.

Because many channels are summed to produce the electron trigger it follows that an energy deposition in a cell adjacent to the one being histogrammed can produce an electron trigger. This would have the effect of adding whatever TDC value is found in the histogrammed channel to fig. 7.ii. This uncertainty contributes to the tails in this histogram.

One example of this uncertainty would be energy leakage into the histogrammed tower from a deposition in an adjacent tower. The magnitude of the resulting signal could be low, and the slew of the discriminator for very small pulse heights would make the time of arrival of the energy appear outside the ToF window. The slew apparent in figure 7.ii is larger than is expected in the final electronics because the discriminator threshold was not set as low as possible.

V. Conclusions

We have implemented a medium scale, fully integrated, pipelined TDC system with 1ns resolution and comprehensive monitoring capabilities, using an ASIC developed for SSC. The variable length pipeline of the ASIC allowed the monitoring facilities to be implemented with minimal overhead.

Because of this integrated implementation, the size and price of the system compares very favourably with a comparable implementation using discrete analogue electronics. For example, in analogue one could probably only integrate a maximum of sixteen channels per module and hence the system would require at least eight crates.

VI. References

[1] The H1 Collaboration, "Technical Proposal to Upgrade the Backward Scattering Region of the H1 Detector", DESY reference PRC 93/02.

[2] Abt et al., "The H1 Detector at HERA", Submitted to NIM.

[3] Y. Arai et al., "A CMOS Four-Channel x 1K Time Memory LSI with 1-ns/b Resolution", in *IEEE Journal of Solid State Circuits*, Vol. 27, No. 3, March 1992, pp 359-364.

[4] Y. Arai et al., "Development of a CMOS Time Memory Cell VLSI and a CAMAC module with 0.5 ns resolution", in *IEEE Transactions on Nuclear Science*, Vol. 39, No. 4, 1992, pp 784-788.