

# The H1 Silicon Tracker

**Benno List**

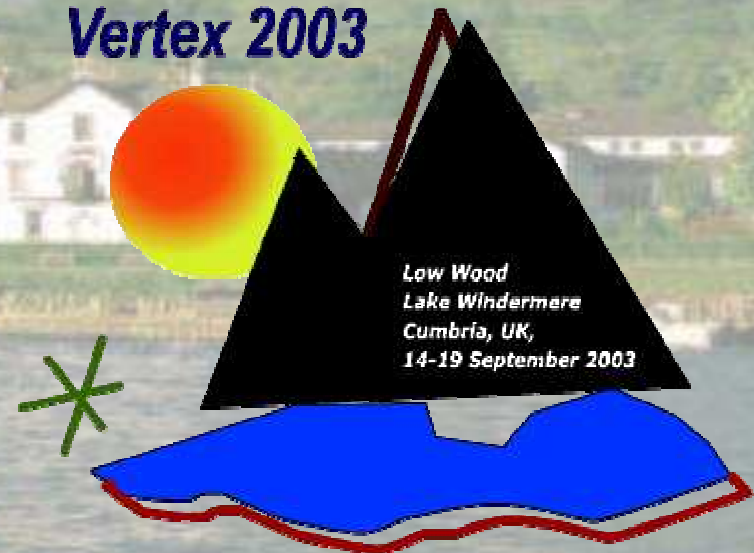


**VERTEX 2003**

15.9.2003

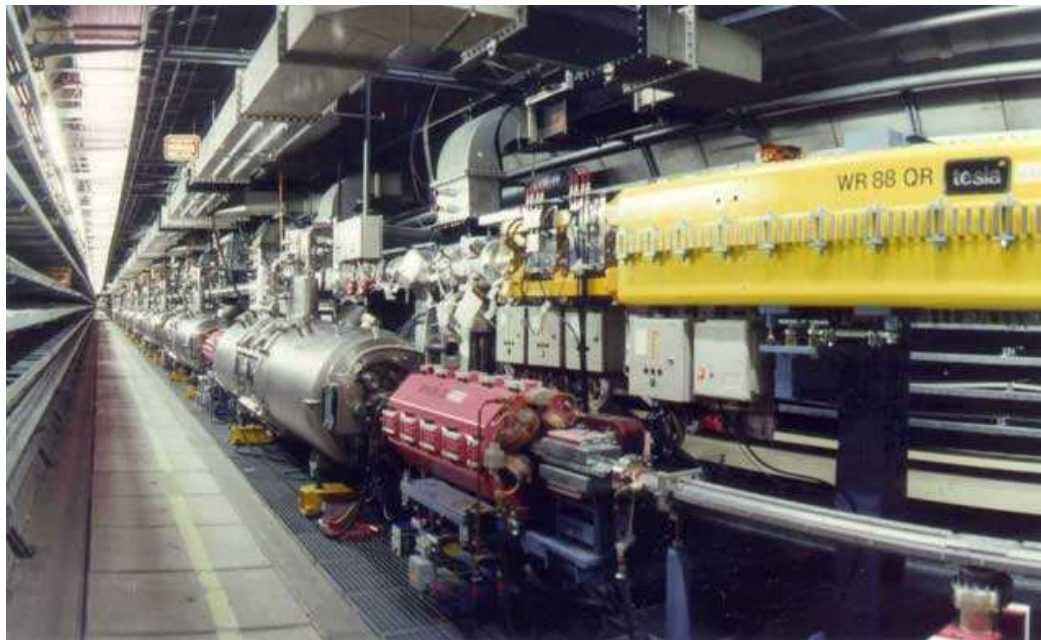
- HERA and H1
- The H1 silicon tracker
- Recent results
- Changes in 2003
- Lessons from the Pit

**Vertex 2003**

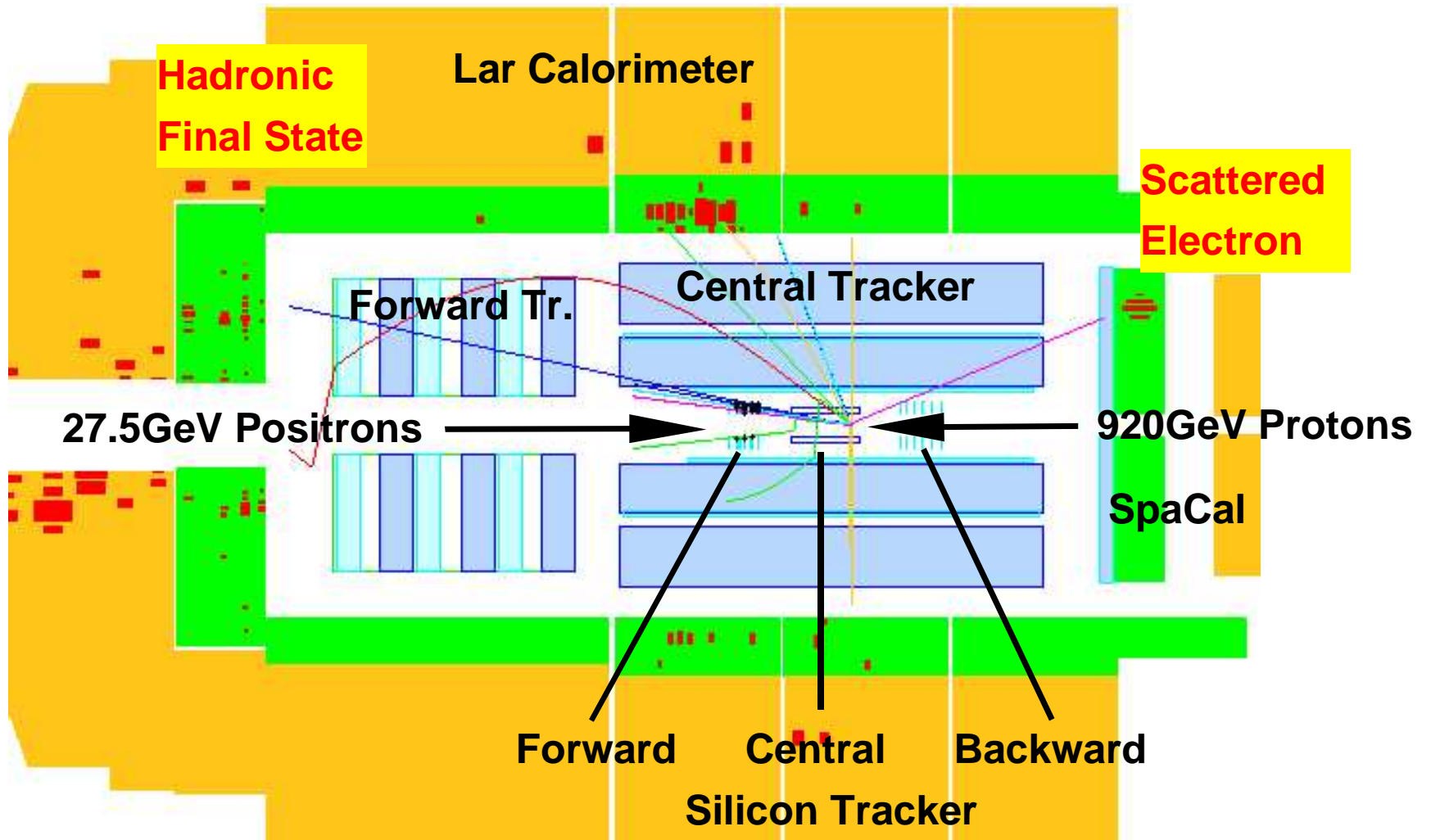


# The HERA ep Collider

- Located at DESY in Hamburg
- 27.5 GeV electrons/positrons on 920 GeV protons
- HERA-I: 1992–2000,  $120\text{pb}^{-1}$
- 2000: Luminosity upgrade
- HERA-II: 2001–2007,  $1000\text{pb}^{-1}$  expected



# The H1 Detector



# Physics Requirements (I)

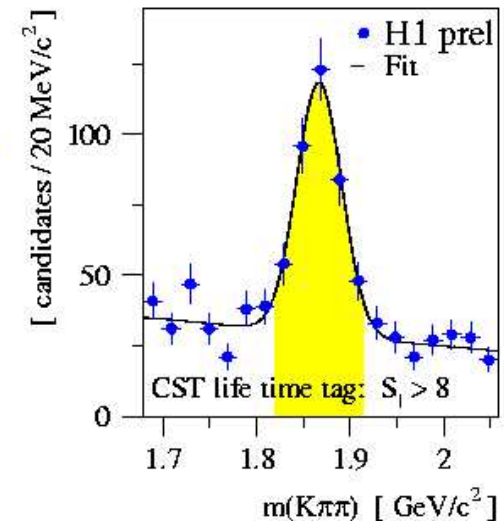
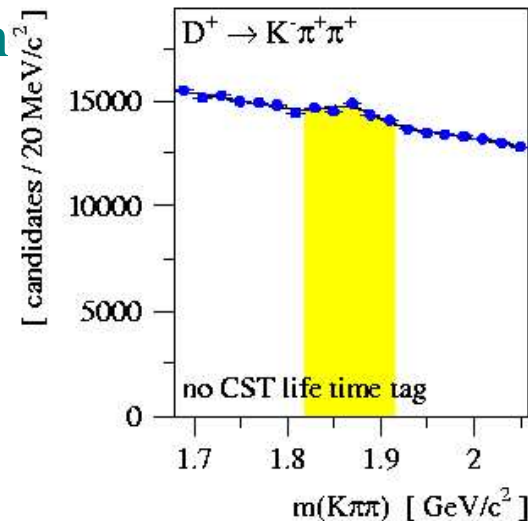
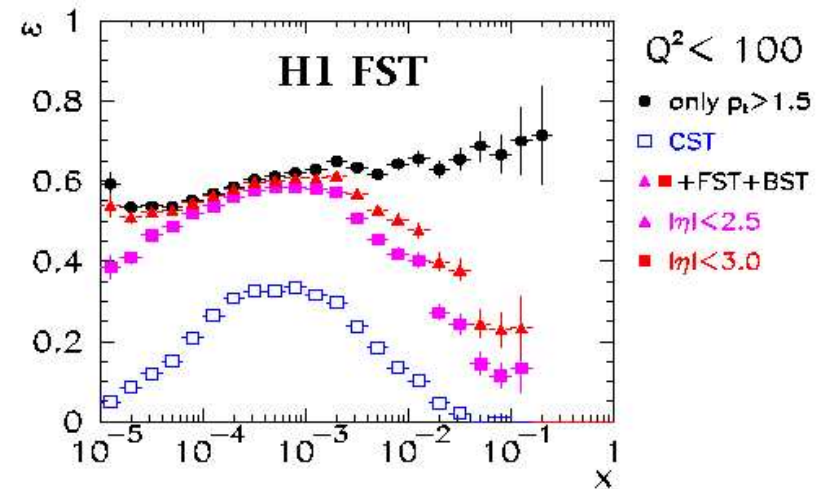
## ● FST:

- Extend tracking (with vertexing capability) into forward direction:  
high track density!  
=> good pattern recognition

## ● CST:

- Provide vertexing capability in central region (charm, beauty)
- Resolution dominated by multiple scattering:  
thin detector!

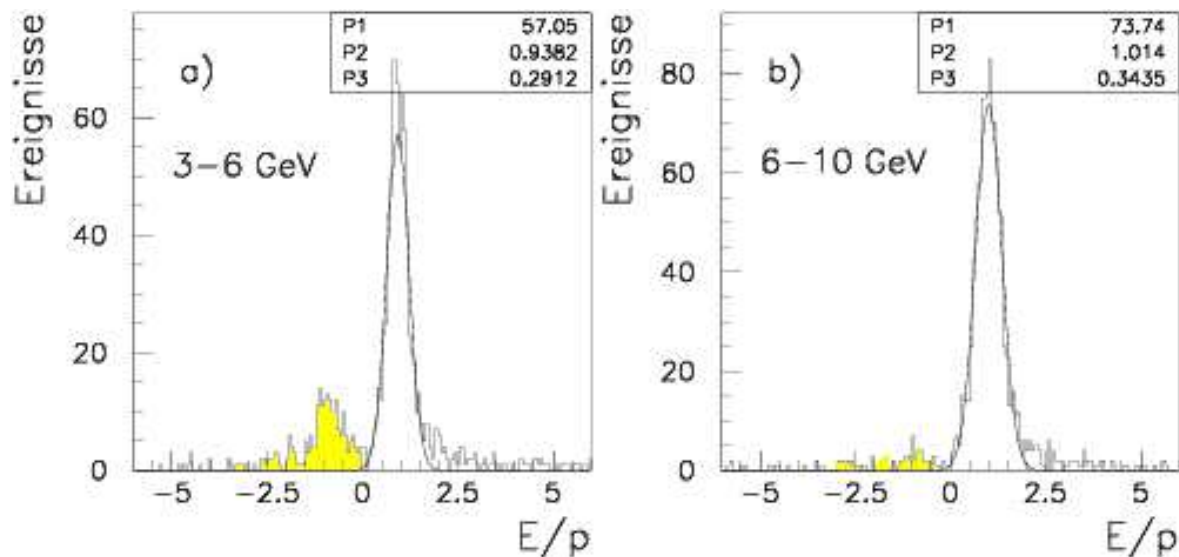
Acceptance of Heavy Quarks  
Deep Inelastic Scattering



# Physics Requirements (II)

## ●BST:

- Measure and trigger scattered electron at low angles:  
suppress fake electrons from  $\pi^0 \rightarrow \gamma\gamma$
- Generally low track density in backward direction



Separation of pions and electrons by measuring energy  $E$  in the calorimeter and momentum  $p$  in BST.

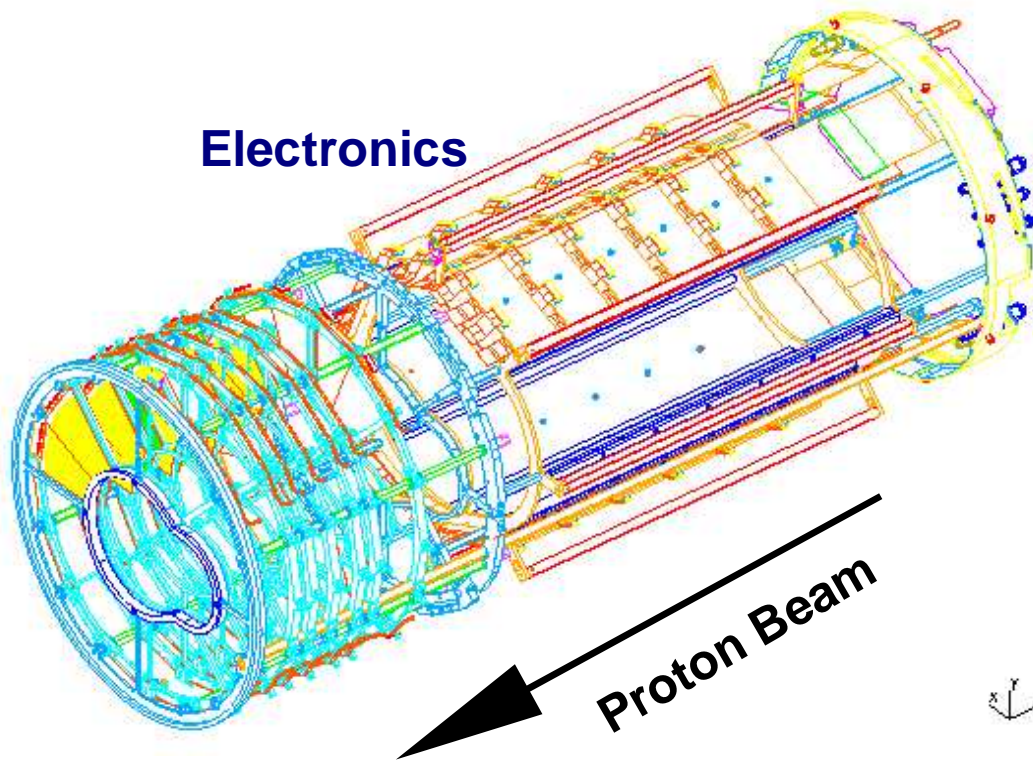
D. Eckstein, DESY-THESIS-2002-8.

# FST: Forward Silicon Tracker

Collaboration of  
DESY–Zeuthen, DESY, Prag, RAL

## Sensor Wheels

## Electronics



## Connectors (Electrical + Cooling)

- 7 sensor wheels,  
2 types: u/v and r
- 3384cm<sup>2</sup> silicon
  - from CIS (Erfurt)
- 92160 channels
- Readout with APC  
(Analog Pipeline Chip)
  - developed at PSI
  - SACMOS: 1.2μm CMOS
  - Manufactured by Faselec

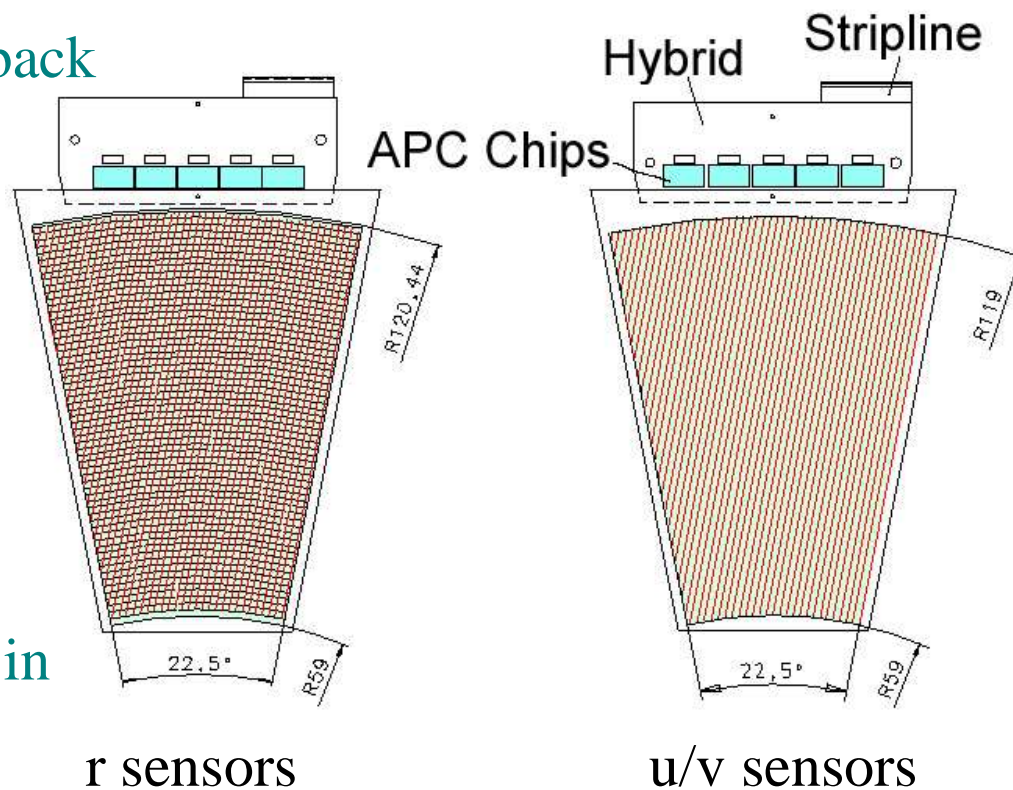
# FST Sensor types

- 5 wheels with u/v coordinate:

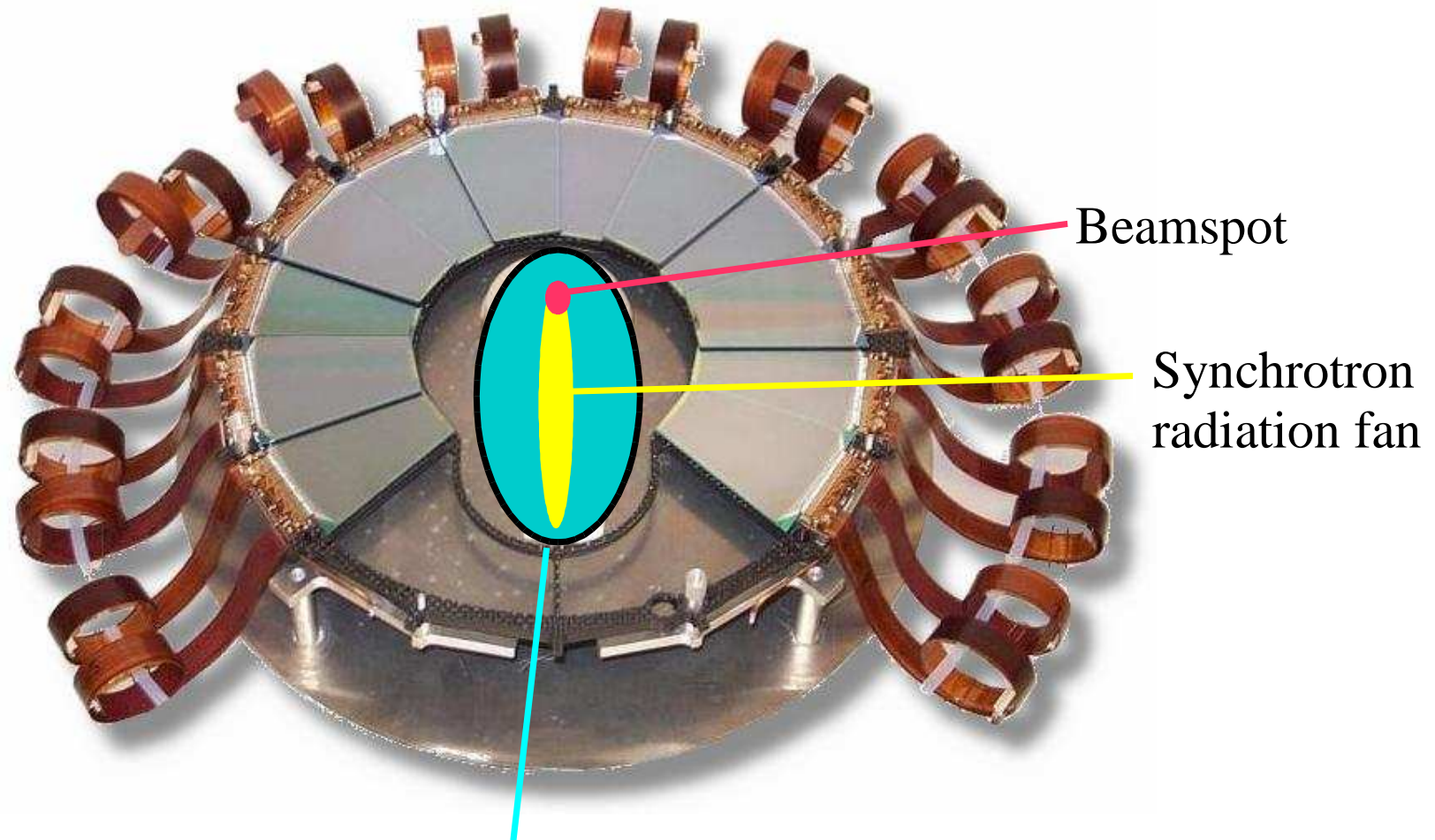
- single sided silicon, back-to-back
- good signal/noise

- 2 wheels with r strips

- single sided silicon
- readout with 2nd metal layer
- reasonable S/N
- needed for pattern recognition in high multiplicity events (ambiguity resolution)



# BST/FST Sensor Wheel



Asymmetric hole to accommodate elliptical beampipe



# FST Performance

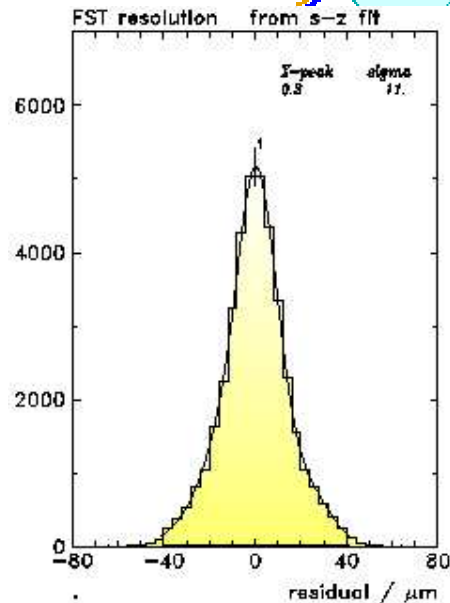
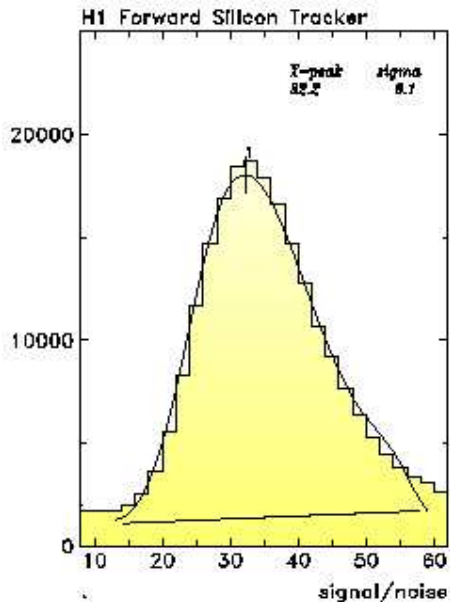
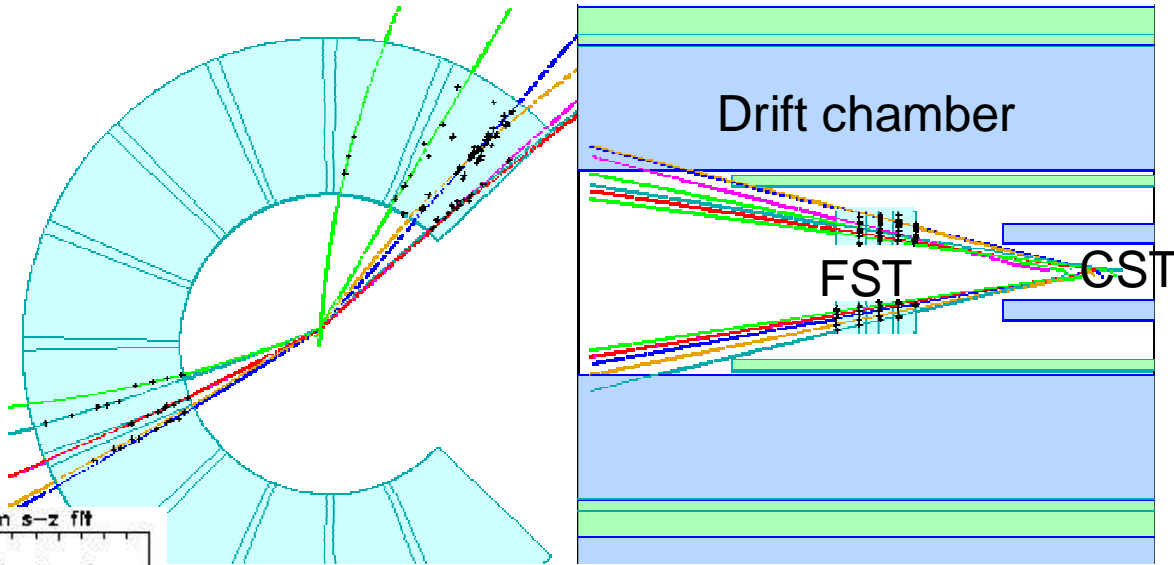
- Signal/Noise:

- 30 for u/v detectors

- 15 for r detectors

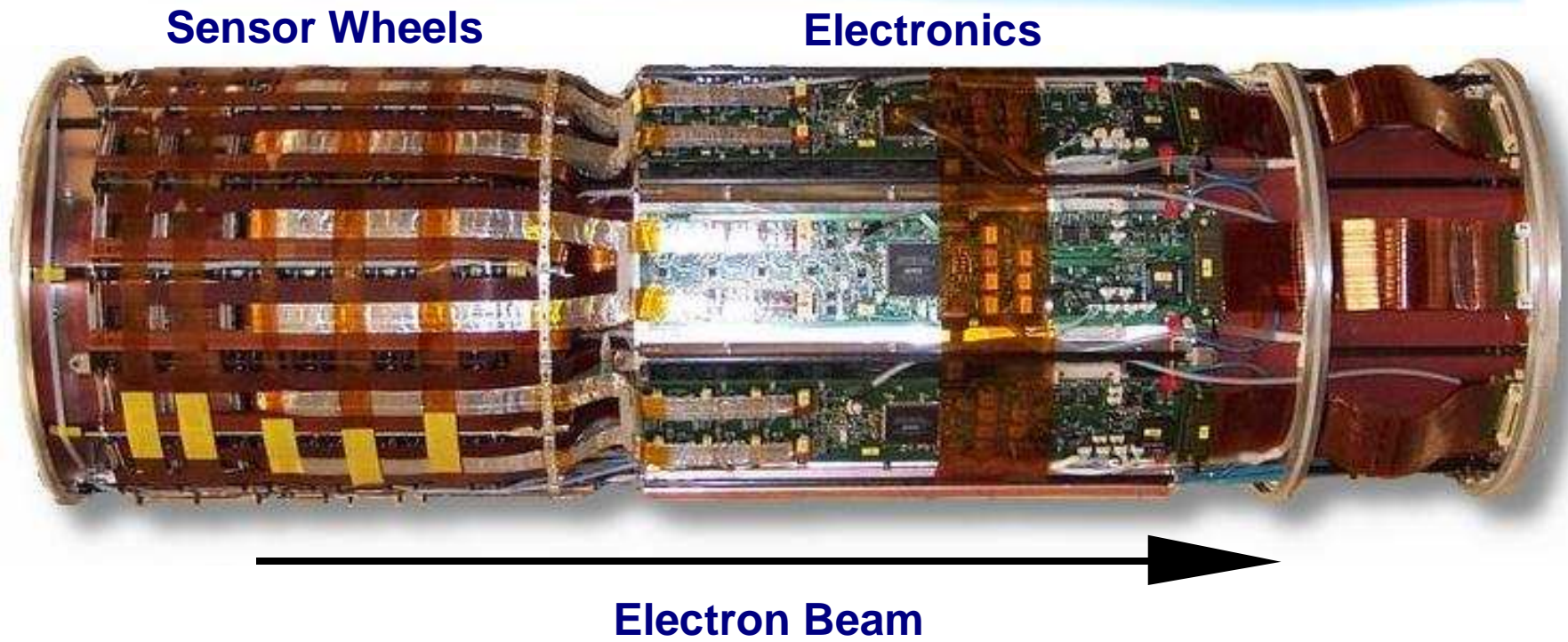
- Resolution  $12\mu\text{m}$   
(from triplet sagitta)

6 tracks in 1  $\phi$  sector



A multitrack event reconstructed in the FST

# BST: Backward Silicon Tracker



- 6 wheels with u/v coordinates, same as in FST: tracking
  - no r wheels needed, typically low multiplicity in backward direction
- 4 wheels with pad detectors: triggering
  - Hit detection + track finding done on frontend, at 10.4MHz

# BST 1, 2, 3

- BST–1: Installed 1995:

- 4 wheels of r detectors  $\times$  16 sensors = 64 sensors, 40960 channels

- BST–2: Upgrade 1998:

- 4 + 4 wheels of r detectors  $\times$  16 sensors = 128 sensors, 81920 channels

- 8 prototype  $\phi$  sensors (u coordinate): 5120 channels

- Upgrade 2001:

- 8 wheels of r detectors  $\times$  12 sensors = 96 sensors, 61440 channels

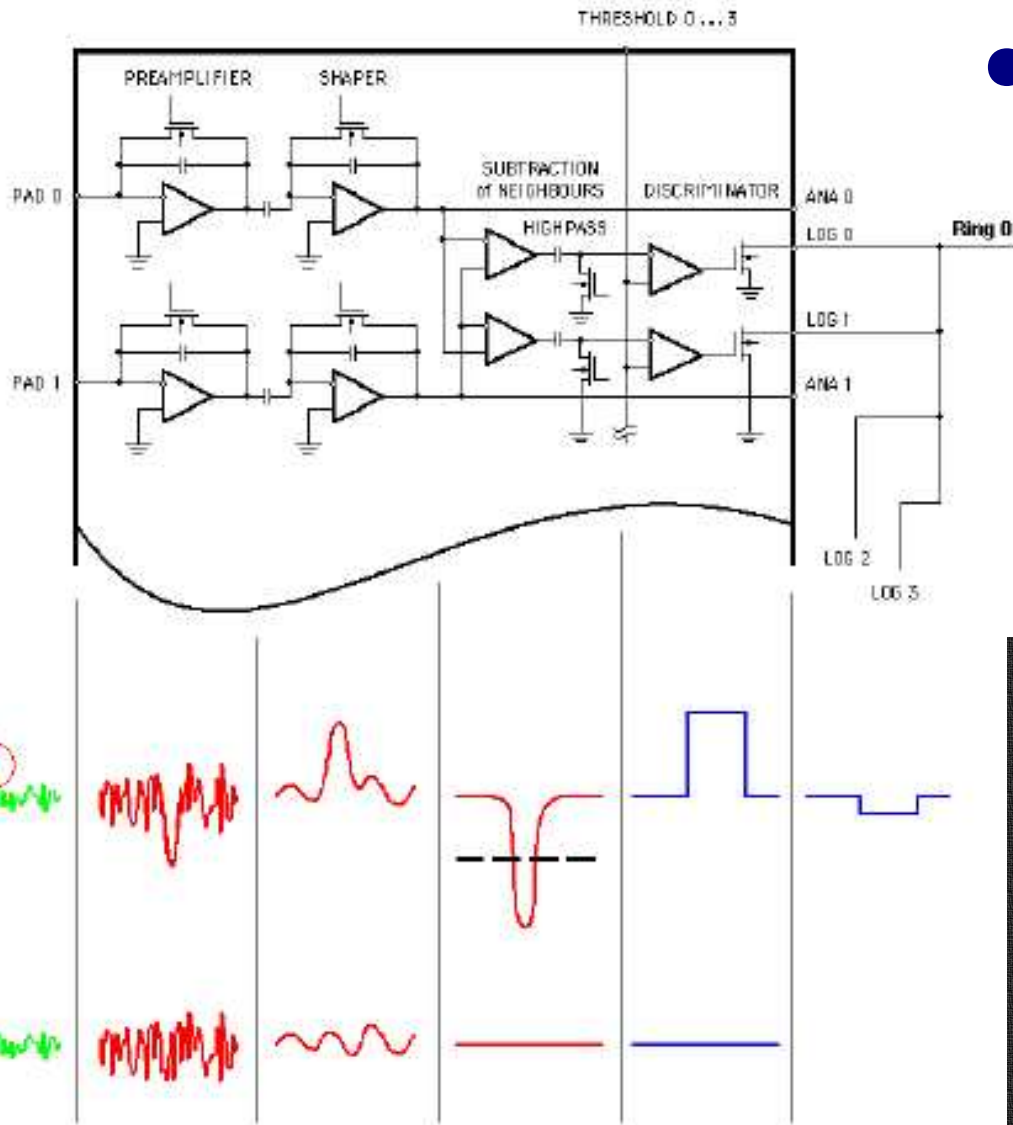
- BST–Pad: 4 wheels of pad detectors  $\times$  12 sensors: 48 sensors, 1536 pads

- BST–3: Upgrade 2003:

- 6 wheels of u/v detectors  $\times$  12 sensors = 132 sensors, 84480 channels

- BST–Pad: 4 wheels of pad detectors  $\times$  12 sensors: 48 sensors, 1536 pads

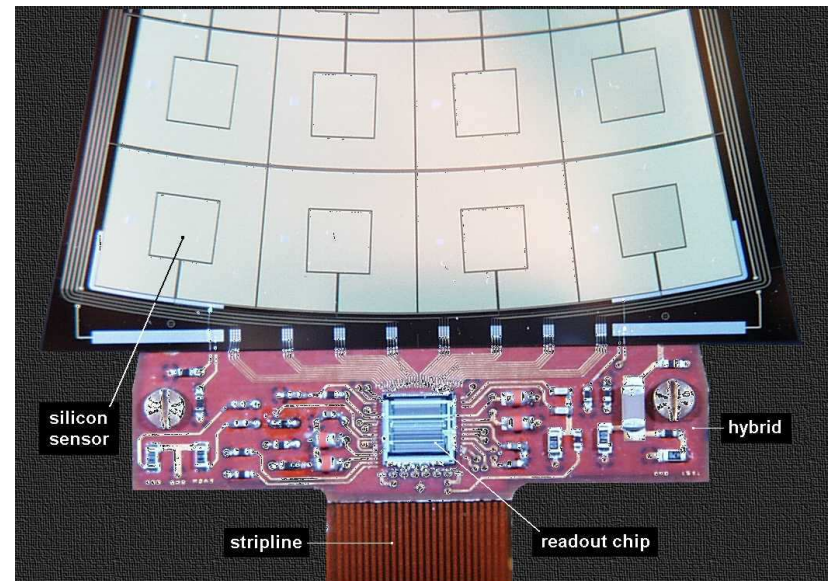
# BST Pad Hit Detection



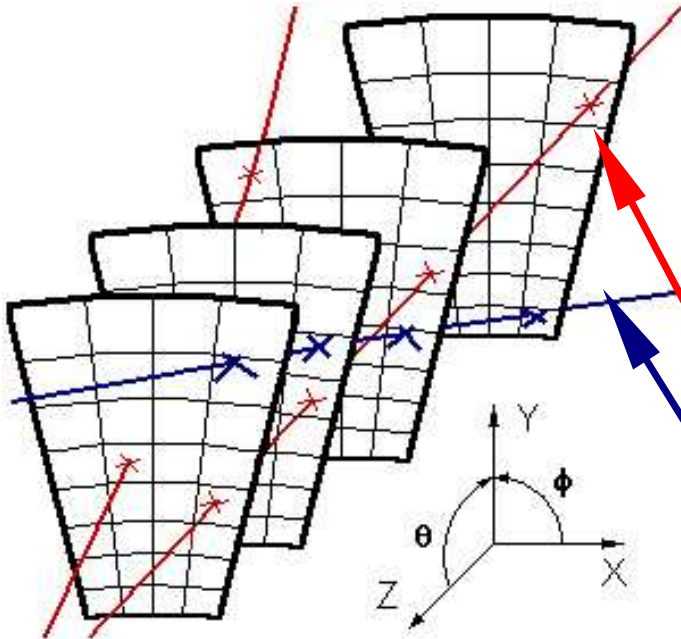
## ● ASIC PRO/A:

- 1.2 $\mu$ m CMOS process
- from IDE AS (Oslo)
- 32 channels per chip
- noise: 600e + 15e/pF
- shaping time 30ns

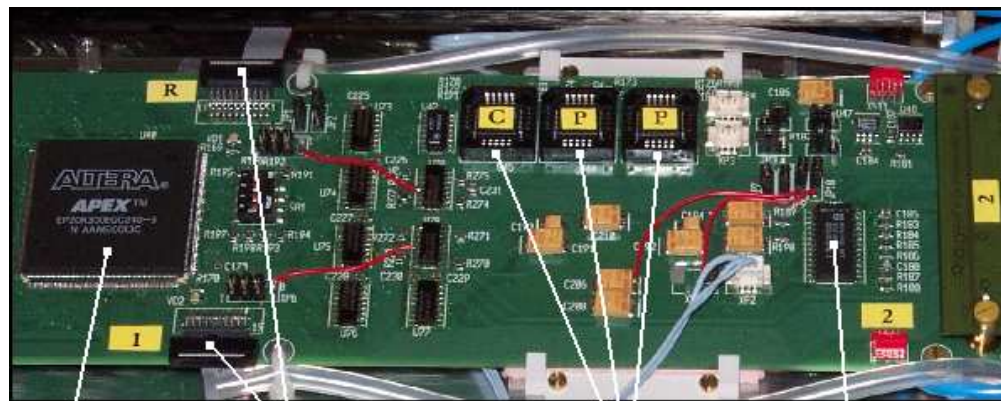
Pad sensors: 8 $\times$ 4=32 pads



# BST Pad Trigger Concept



- One motherboard for 2 sectors (8 sensors), mounted directly behind sensor volume
- Complex Programmable Logic Devices (CPLDs) from ALTERA for trigger
  - Recognises tracks from IP
  - Rejects tracks from outside interaction region
  - Flexible, for shifted vertex runs



CPLD  
(data proc.)

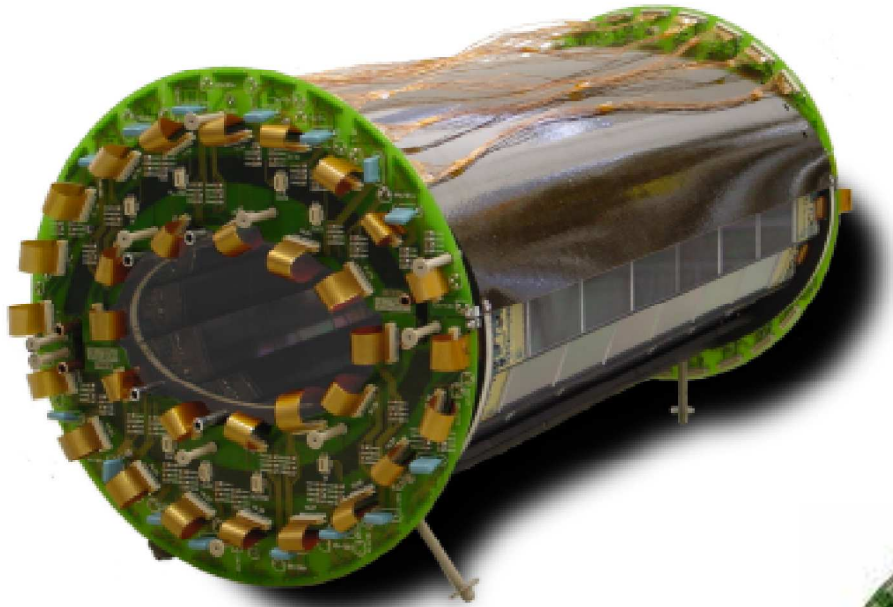
Link to other  
 $\phi$  sectors

"Power ON"  
configuration

User access  
interface

- Uses Content Adressable Memory (CAM) to compare hit patterns with predefined hit patterns from tracks

# The CST



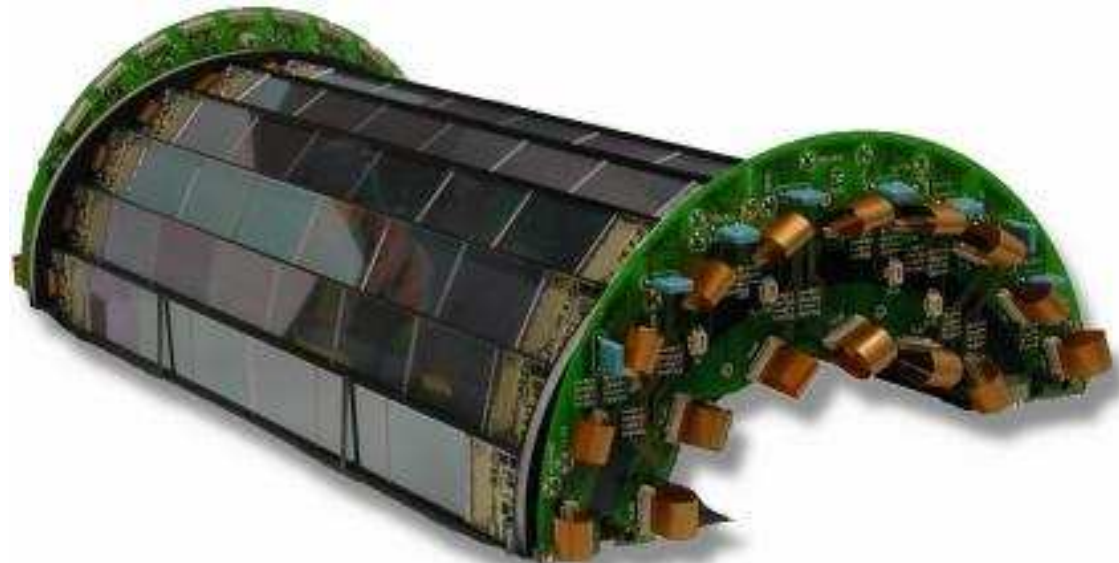
- 2 barrel layers, 12+20 ladders
- 192 sensors  $3.4 \times 5.9 \text{ cm}^2$
- $3850 \text{ cm}^2$  silicon
- 3 sensors read out together
- 81920 channels
- Very thin:  $1.4\% X_0$  in radial direction

- Analog readout with rad-hard DMILL APC

➤ manufactured by ATMEL

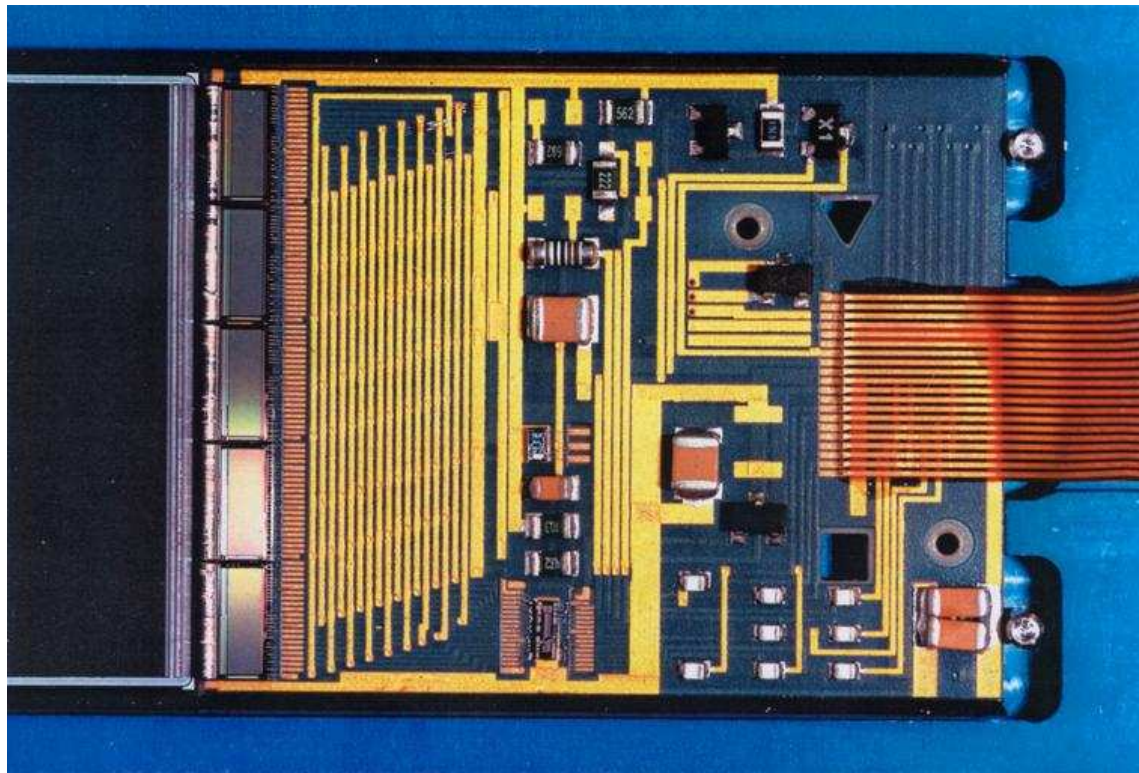
- Optical signal transmission

Built by ETH Zurich, PSI, Uni. Zurich, DESY, RAL

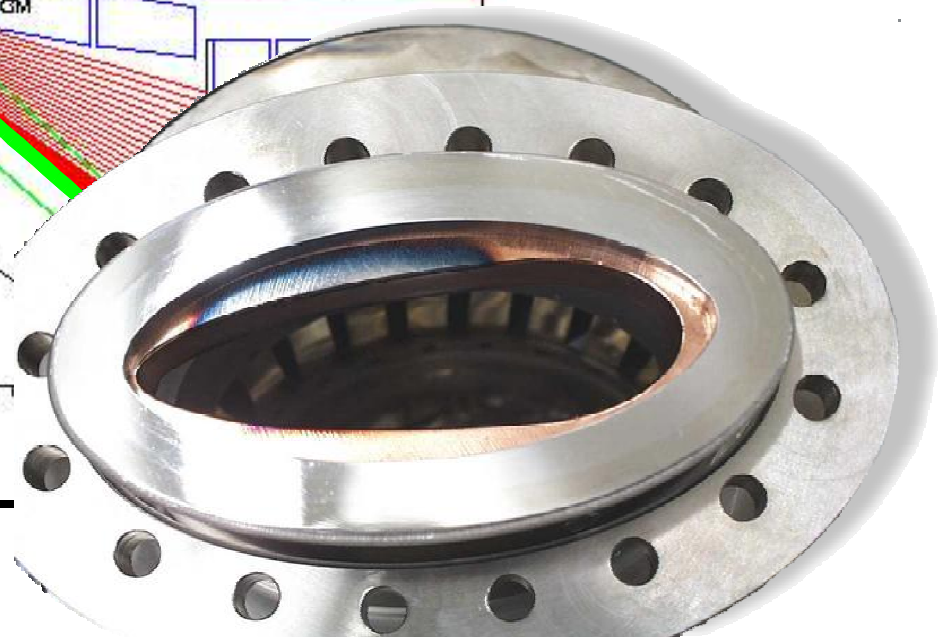
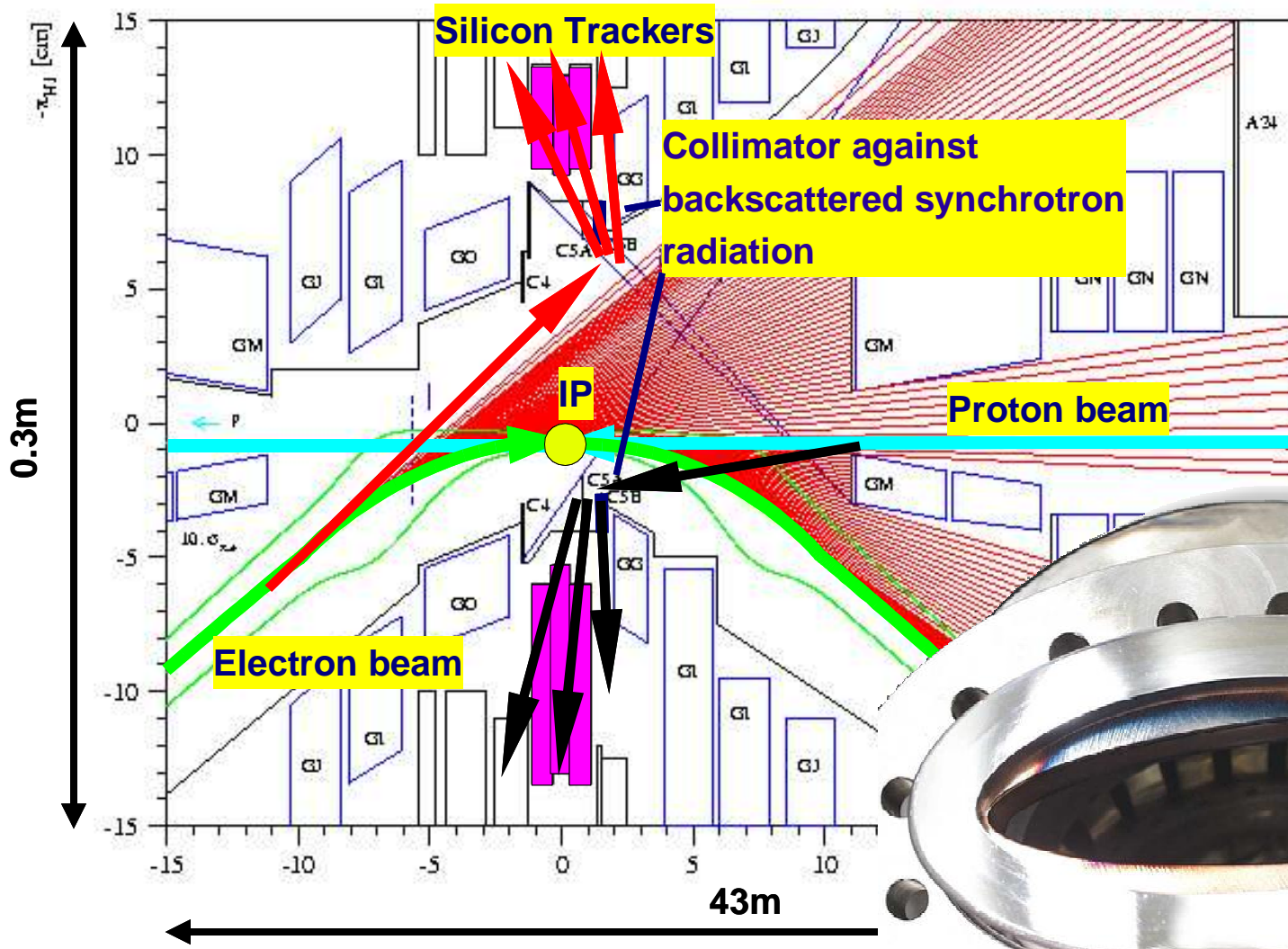


# Shutdown Work on CST

- March–June 2003: 17 weeks shutdown
- CST: Repairs, upgrade to radhard readout:
  - Last 12 of 64 half ladders were equipped with radiation hard (DMILL) readout chips; now all CST readout ASICs are DMILL chips



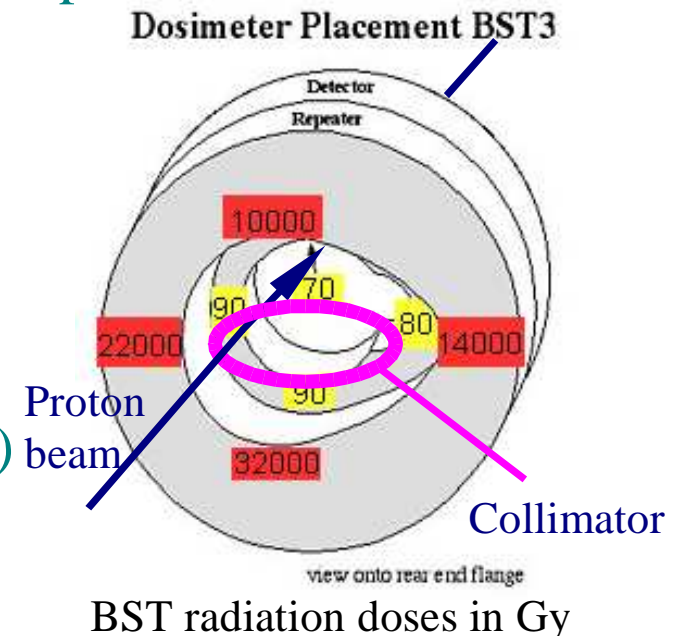
# Backgrounds





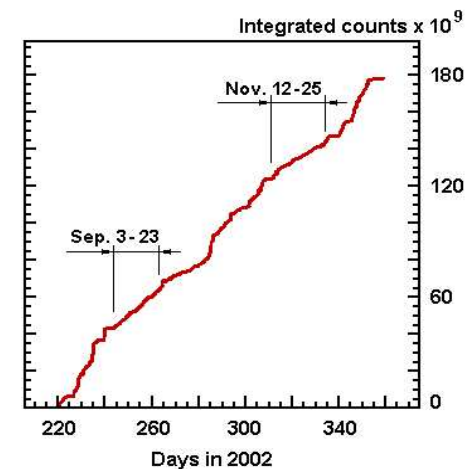
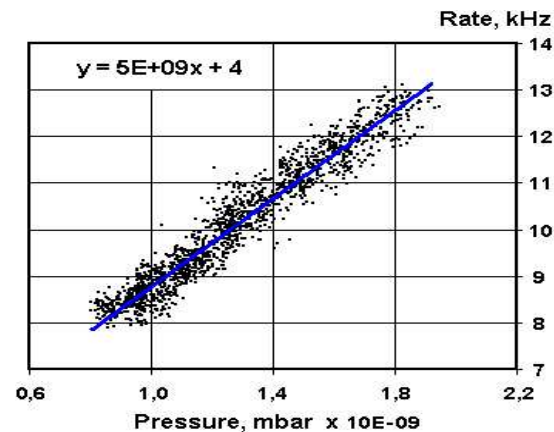
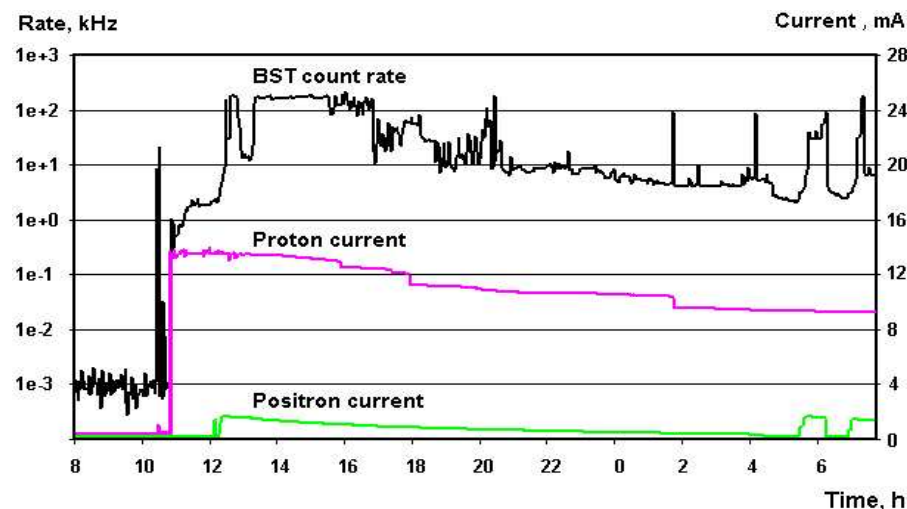
# Radiation Damage to BST

- Dosimeters in BST showed up to 30kGy of dose
- High dose only in small region at  $-z$  end (around collimator), FST, CST, forward region of BST received  $<100\text{Gy}$
- Damages:
  - APC chips of BST: do not hold charge long enough (1ms) for readout (same problem lead to installation of radhard chips in CST)
  - BST slow control circuitry damaged
  - line receivers, drivers damaged
  - ALTERA CPLD chips survived!
  - Voltage regulators for CST damaged (located at same  $z$  position as BST electronics)



# Beam optimization using BST Pad Rates

- Use single pad rate to monitor beam conditions
- Very useful for beam tuning
- Problem:
  - Large background spikes (from beam missteering) deprogram CPLDs
- This was an unforeseen application, shows advantage of CPLDs:  
can be easily adapted to new demands



# Summary

- HERA-II had a slow start, but is now on track
- Radiation damage occurred mainly from an incident where synchrotron radiation directly hit a collimator
- Normal operation of HERA leads to doses  $\sim 100\text{Gy/y}$
- BST and CST have been repaired
- CST now fully equipped with DMILL chips
- Looking forward to next data taking