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New TOF DAQ status

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Brief description

The signals from TOF PMs (after discriminators) and gate signals are fed to multihit TDCs and PTL2000 modules. Time measurements from the TDC and scalers of PTL2000 are readout by RIO2 VME CPU under LynxOS operating system. Then banks are sent to ETAG DAQ branch and, in parallel, prescaled event data are sent to the slowcontrol PC.

Tests on real data

The operation of digitizer modules (PTL2000 and CAEN TDC V767) is tested on real (BTS and some gates) data. The PTL2000 up to now showed no problems. The TDC operates with glitches – data loss, output buffer lockup. Have to be studied further.

Changes since the last report

Found an error in measured overheads of system calls and IRQ latency. It appeared that the use of printf() in a program introduces some hidden delays (10-15μs) in scheduling points of the program (additional hidden threads in LynxOS ?). The new numbers are: IRQ to CPU response time is around 10μs (from wait state), switching to another process thread takes 8μs, reenabling IRQ takes 25μs.

All necessary custom made modules - level translators (NIM to Diff. ECL and NIM to H1-standard) have been made (V.Volchinsky). There are plans to modify NIM to Diff. ECL translator modules so that the input signals can be inhibited. This is necessary for TOF gates measurement by multihit TDC, since the gates come in 10 MHz frequency (TDC L1 buff. overflow). The solution is found by V.Volchinsky and the work on the modifications will start soon.

The new TOF DAQ electronics, for the duration of the shutdown, is moved to the building 10b for detailed tests of TDC and simulation of ETAG branch to the TOF DAQ communication via dual-ported memory.

Plans

Tests of the TDC in a more convenient place.

Development and debugging of the communication algorithm between TOF DAQ and ETAG branch via dual-ported memory.